Kansas Fest 93

Session: Digital Electronics

Presenter: Chuck Kelly / ProDev, Inc.

Basic Electronics Review

It may help in your understanding of electricity if you compare it to fluid flowing in pipes.

Electricity	Fluid
Voltage	PSI pressure in a water pipe.
Current	Flow rate (Gallons Per Minute)
Resistance	Flow restrictor

$$\text{Ohm's Law} = \frac{E}{I \mid R}$$

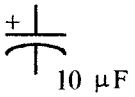
E = Voltage in (Volts)
I = Current in (Amps)
R = Resistance in (Ohms)

Voltage - Force that is being excerted on the electrons
Symbol : "E" or "V"
Unit : "volt"

Current - Flow rate of the electrons.
Unit : "Amp"
Symbol : "I"

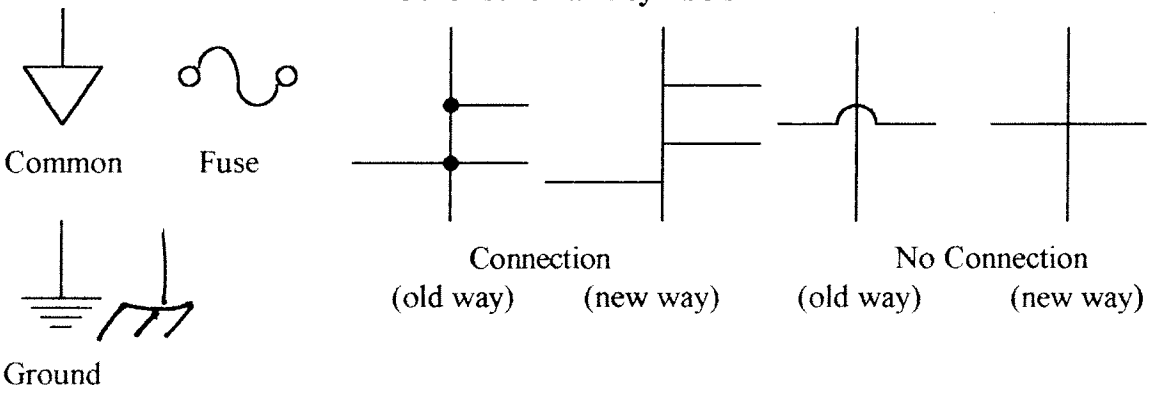
Resistance - Resistance to the flow of electrons.
Unit : "Ohm"
Symbol : "Ω"

Capacitor - Block the flow of Direct Current and pass the flow of Alternating Current.
Term : "Capacitance"
Unit : "Farad".
Symbol : "F"



Inductor - Block the flow of Alternating Current and pass the flow of Direct Current.
Term : "Inductance"
Unit : "Henry"
Symbol : "H"

Other schematic symbols



Transistor transistor Logic

TTL logic levels

```
        5V
         :      Logic 1
        2V
-----------------------------------
         :
Undefined logic level
         :
-----------------------------------
       0.8V
         :      Logic 0
       0.0V
```

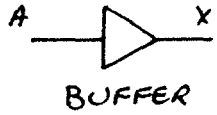
Binary, Hex, BCD

Decimal	Binary	BCD	Hex
0	0000	0000	00
1	0001	0001	01
2	0010	0010	02
3	0011	0011	03
4	0100	0100	04
5	0101	0101	05
6	0110	0110	06
7	0111	0111	07
8	1000	1000	08
9	1001	1001	09
10	1010	0001 0000	0A
11	1011	0001 0001	0B
12	1100	0001 0010	0C
13	1101	0001 0011	0D
14	1110	0001 0100	0E
15	1111	0001 0101	0F
16	10000	0001 0110	10

ASCII

Character	ASCII code (Hex)
A	41
B	42
:	:
Z	5A

GATES



BUFFER

Ø IN Ø OUT

1 IN 1 OUT

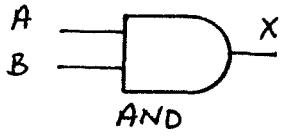
$X = A$

INVERTER

Ø IN 1 OUT

1 IN Ø OUT

$X = \overline{A}$

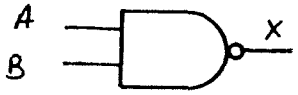


AND

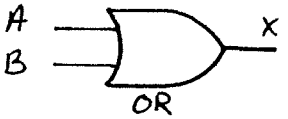
A	B	$X = A \cdot B$
0	0	0
0	1	0
1	0	0
1	1	1

NAND

$X = \overline{A \cdot B}$
1
1
1
0



NAND



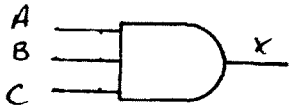
OR

A	B	$X = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

NOR

$X = \overline{A + B}$
1
0
0
0

NOR



AND

BOOLEAN

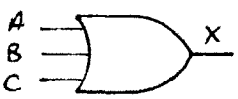
$X = A \cdot B \cdot C$

OR

$X = ABC$

AND

A	B	C	$X = A \cdot B \cdot C$
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1



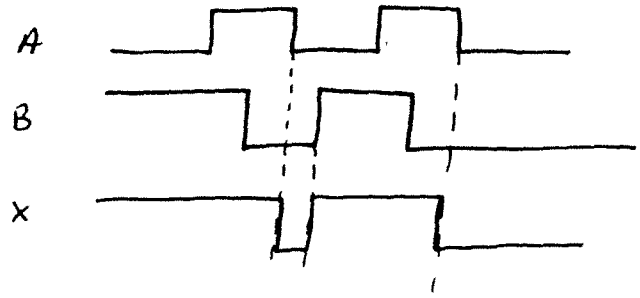
OR

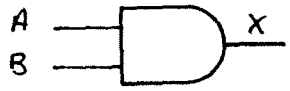
OR

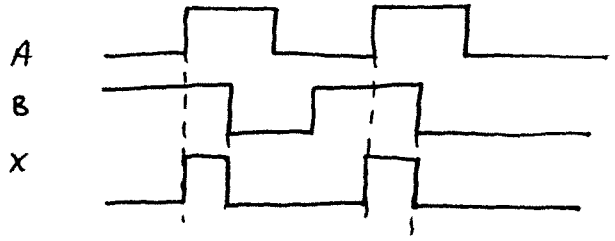
A	B	C	$X = A+B+$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

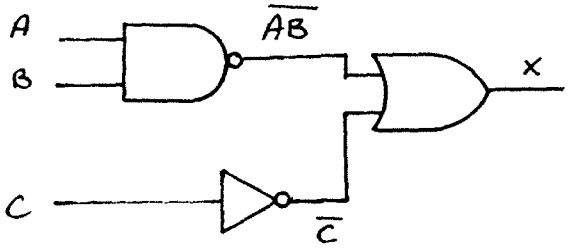
BOOLEAN

$X = A + B + C$

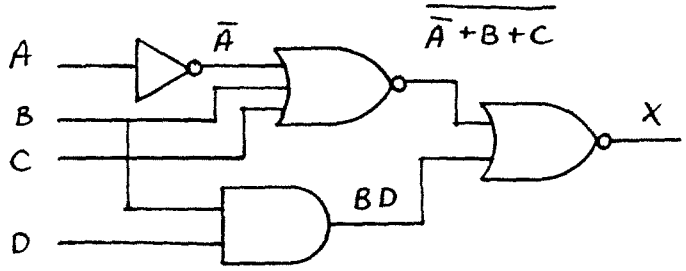




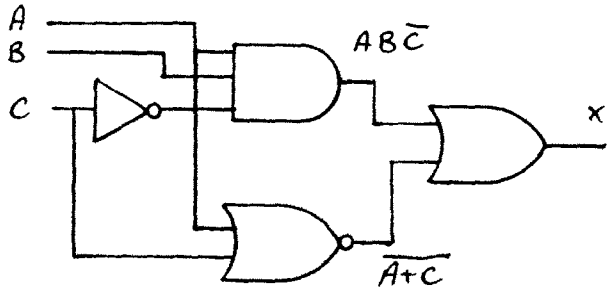




$X = \overline{AB} + \overline{C}$



$X = \overline{\overline{A+B+C} + BD}$



$X = AB\overline{C} + (\overline{A+C})$

BOOLEAN THEOREMS

$X \cdot 0 = 0$ $\quad X + 0 = X$ $\quad \overline{\overline{X}} = X$

$X \cdot 1 = X$ $\quad X + 1 = 1$

$X \cdot X = X$ $\quad X + X = X$

$X \cdot \overline{X} = 0$ $\quad X + \overline{X} = 1$

$X + Y = Y + X$

$X \cdot Y = Y \cdot X$

$X + (Y + Z) = (X + Y) + Z = X + Y + Z$

$X (YZ) = (XY) Z = XYZ$

$X (Y + Z) = XY + XZ$

$(W + X)(Y + Z) = WY + XY + WZ + XZ$

$X + XY = X$

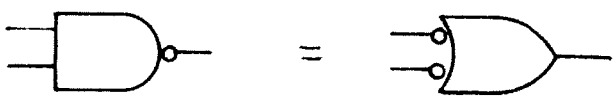
$X + \overline{X} Y = X + Y$

DE MORGAN'S THEOREMS

$\overline{X + Y} = \overline{X} \cdot \overline{Y}$ $\quad \overline{\overline{X} + \overline{Y}} = X \cdot Y$

$1 \quad 0 = 0$ $\quad 1 \quad 0 = 0$

$\overline{X \cdot Y} = \overline{X} + Y$ $\quad \overline{\overline{X} \cdot \overline{Y}} = X + Y$



BOOLEAN ALGEBRA EXAMPLES

#1 $\overline{A + \overline{BC}} + ABC$

DEMORGANS

$\bar{A}BC + ABC$

FACTOR OUT COMMON BC

$BC(\bar{A} + A)$

$X + \bar{X} = 1$

$BC(1)$

$X \cdot 1 = X$

$\boxed{BC}$

#2 $(A + BC)(AC + \bar{B})$

$A\cancel{A}C + A\bar{B} + ABC\cancel{C} + B\cancel{\bar{B}}C$

$AC + (A\bar{B} + ABC) + 0$

$AC + A(\bar{B} + BC)$

$AC + A(\bar{B} + C)$

$AC + A\bar{B} + \cancel{AC}$

$\boxed{AC + A\bar{B}}$

#3 $\bar{A} + \bar{B} + \bar{C} + \bar{A}\bar{B}\bar{C} + ABC$

$\overline{ABC} + \bar{A}\bar{B}\bar{C} + ABC$

$\bar{A}\bar{B}\bar{C} + (\cancel{ABC + \overline{ABC}})$

1

$\bar{A}\bar{B}\bar{C} + 1$

$\boxed{1}$

#4 $\left(\overline{\overline{A+B} \cdot \overline{B+C}}\right) \cdot \left(\overline{\overline{BC} + \overline{CD}}\right)$

$[(A+B) + (B+C)] \cdot [BC \cdot CD]$

$(A + (B + \cancel{B}) + C)(BCD)$

$(A + B + C)(BCD)$

$ABCD + \cancel{B}BCD + BC\cancel{C}D$

$ABCD + (BCD + BCD)$

$ABCD + BCD$

$BCD(\cancel{A} + 1)$

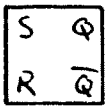
$\boxed{BCD}$

X = DON'T CARE

Q_0 = PRIOR STATE OF Q OR NO CHANGE

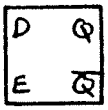
FLIP-FLOPS

SR LATCH



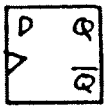
S	R	Q
0	0	NO CHANGE
1	0	Q = 1
0	1	Q = 0
1	1	INVALID

D LATCH



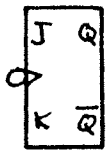
E	D	Q
0	X	Q_0
1	0	0
1	1	1

D F-F

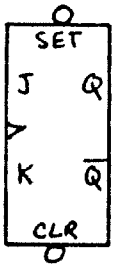


D	CLK	Q
0	↑	0
1	↑	1

JK F-F



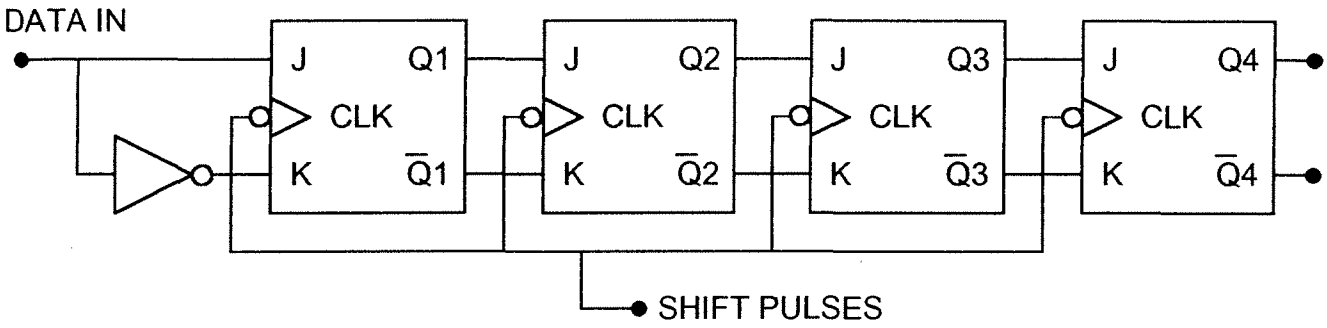
J	K	CLK	Q
0	0	↓	Q_0
1	0	↓	1
0	1	↓	0
1	1	↓	$\overline{Q_0}$ (TOGGLES)

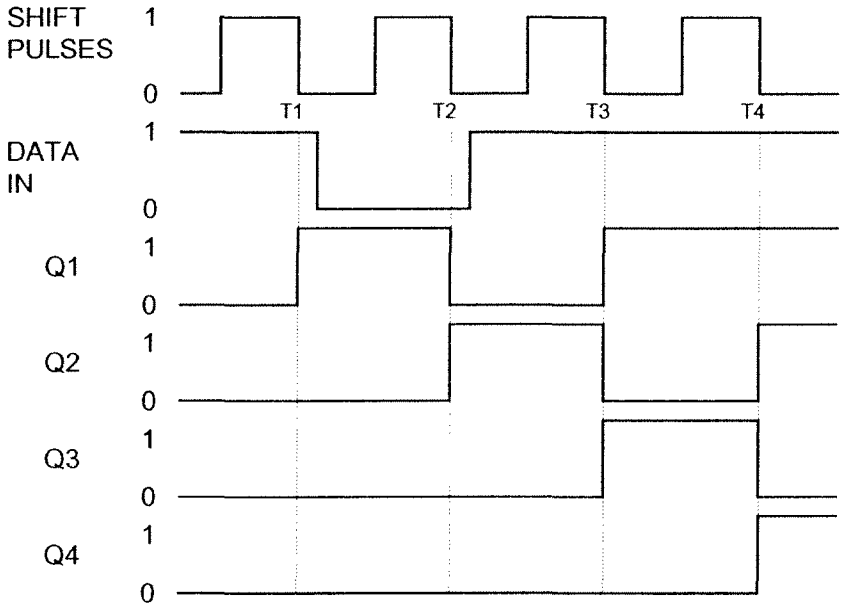


SET	CLR	RESPONSE
1	1	NORMAL OPERATION
0	1	Q = 1
1	0	Q = 0
0	0	NOT USED

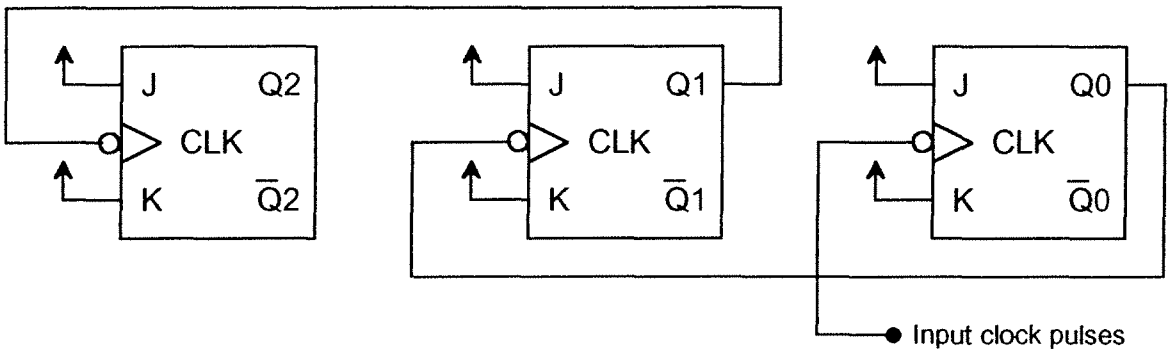
ASYNCHRONOUS SET & CLEAR

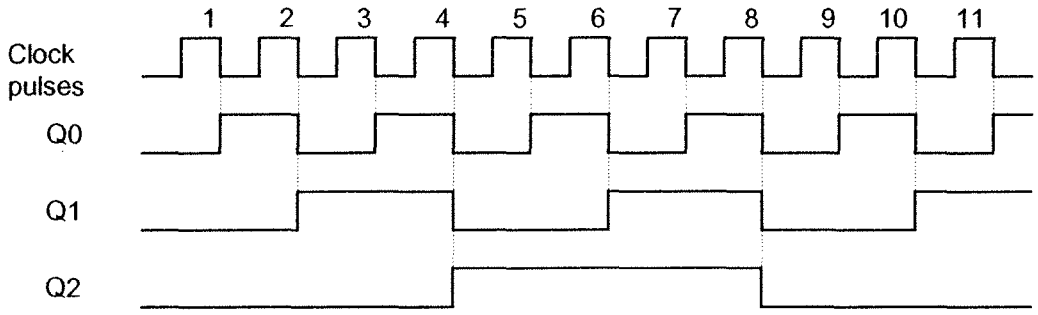
FOUR BIT SHIFT REGISTER





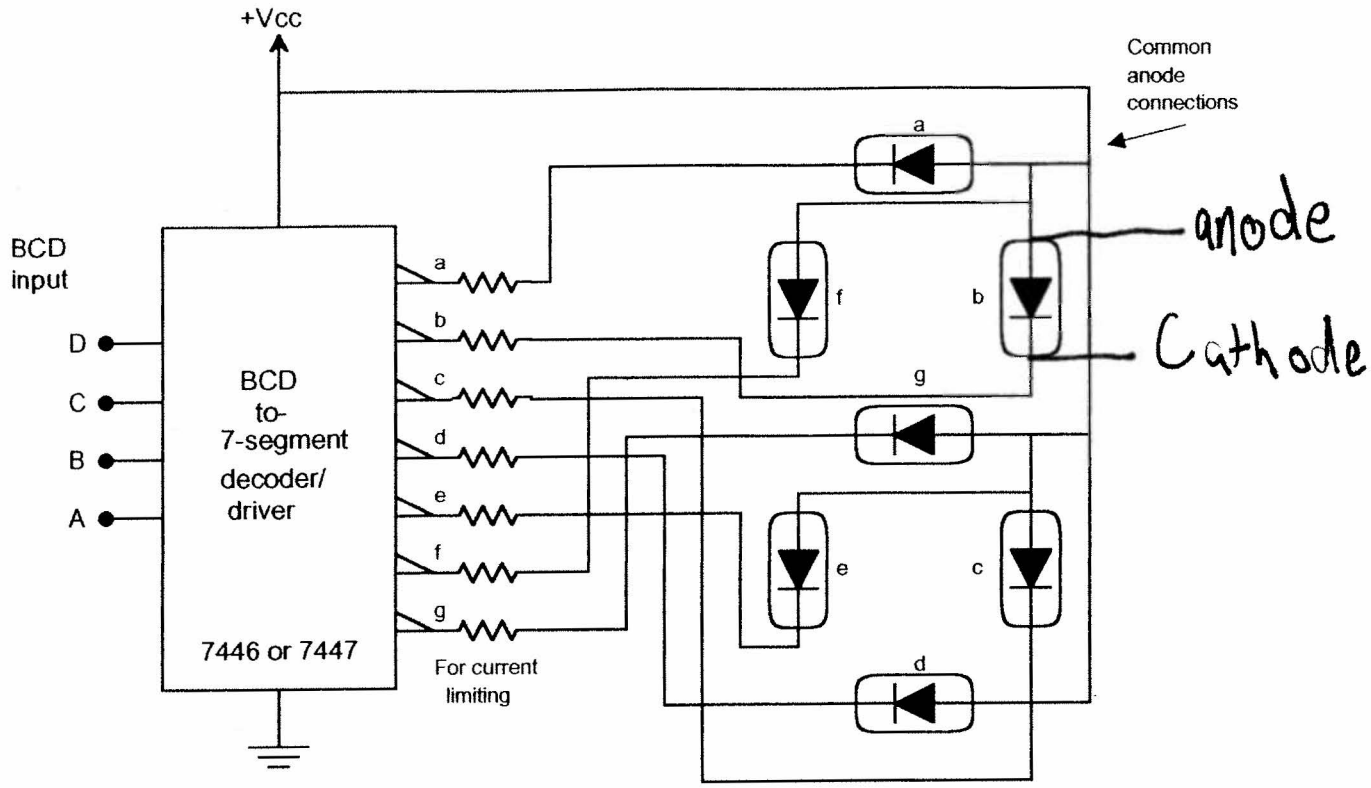
COUNTER

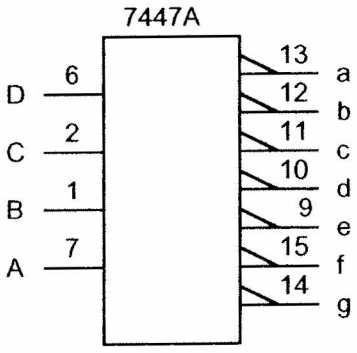




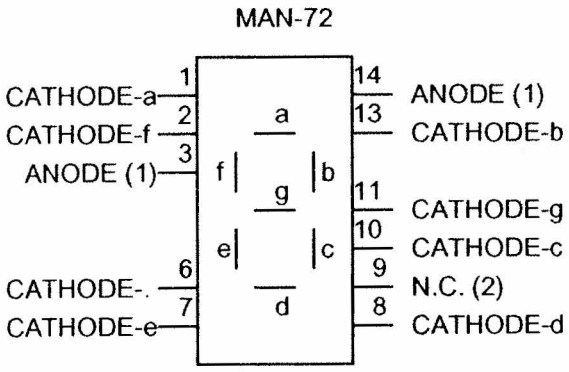
Flip-flops wired as a 3-bit binary ripple counter (MOD-8).

2	1	0	Clock pulse
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7
0	0	0	8

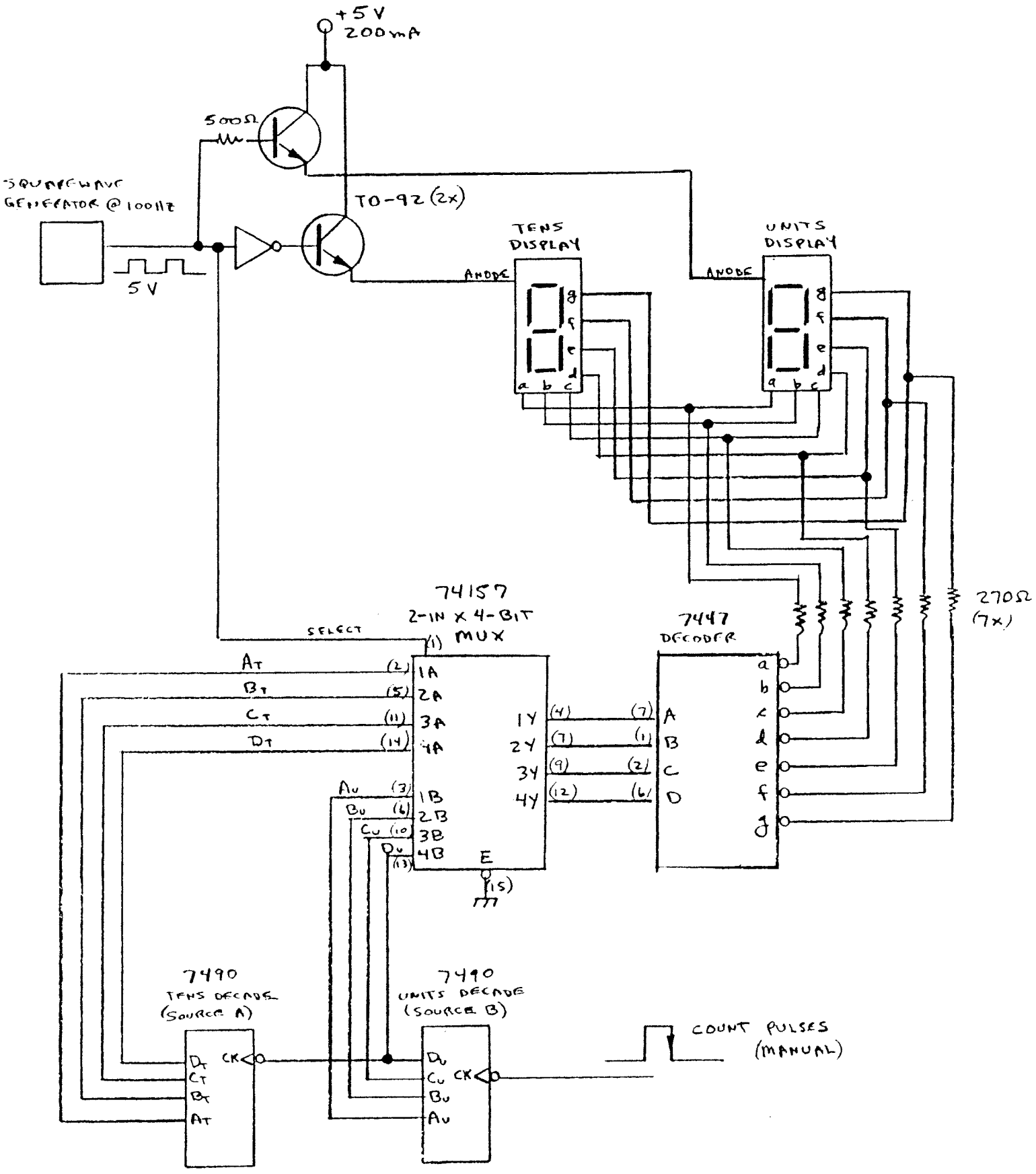




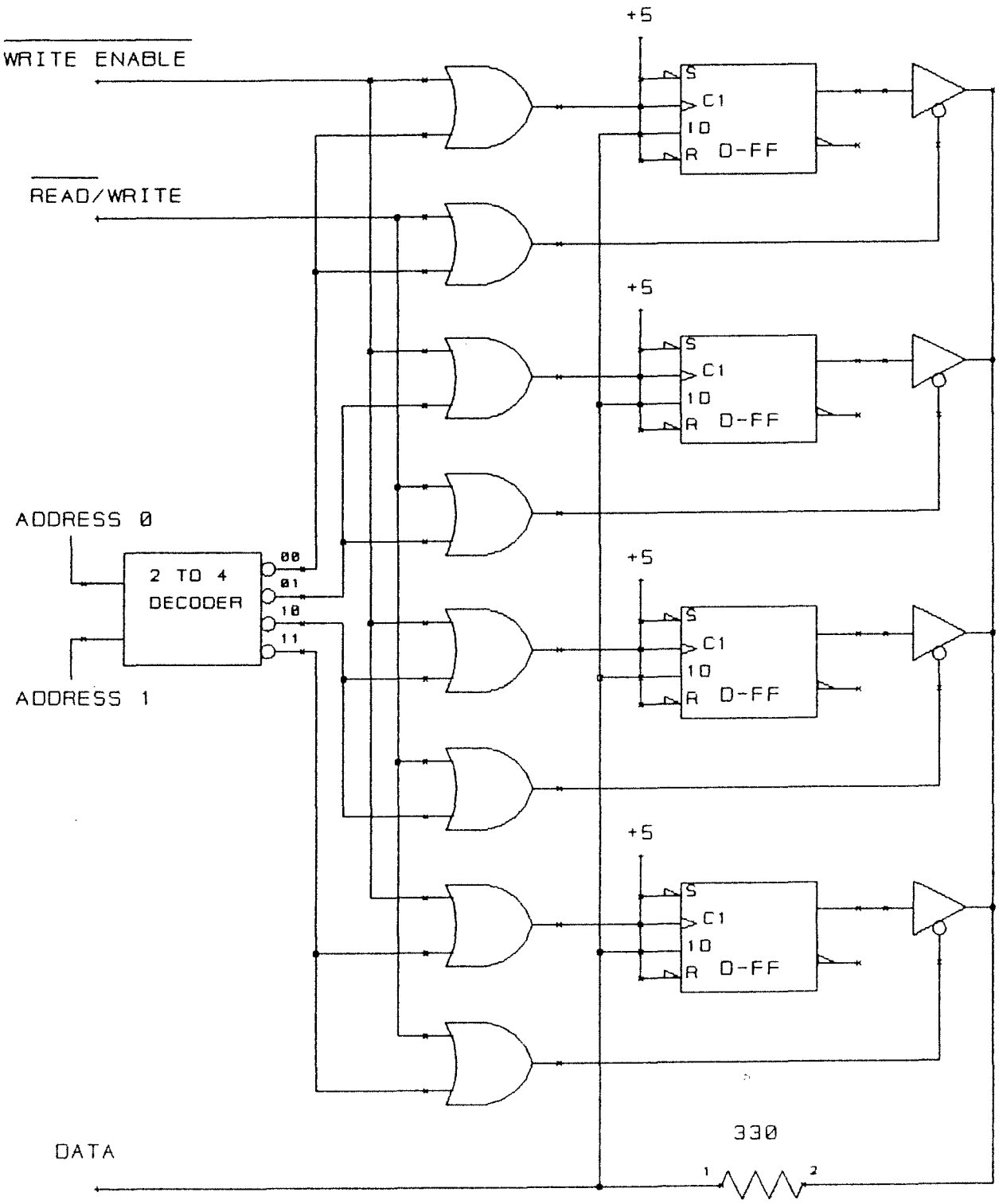
Vcc 16
GND 8



NOTES
1 Redundant anodes
2 Leave pin unconnected

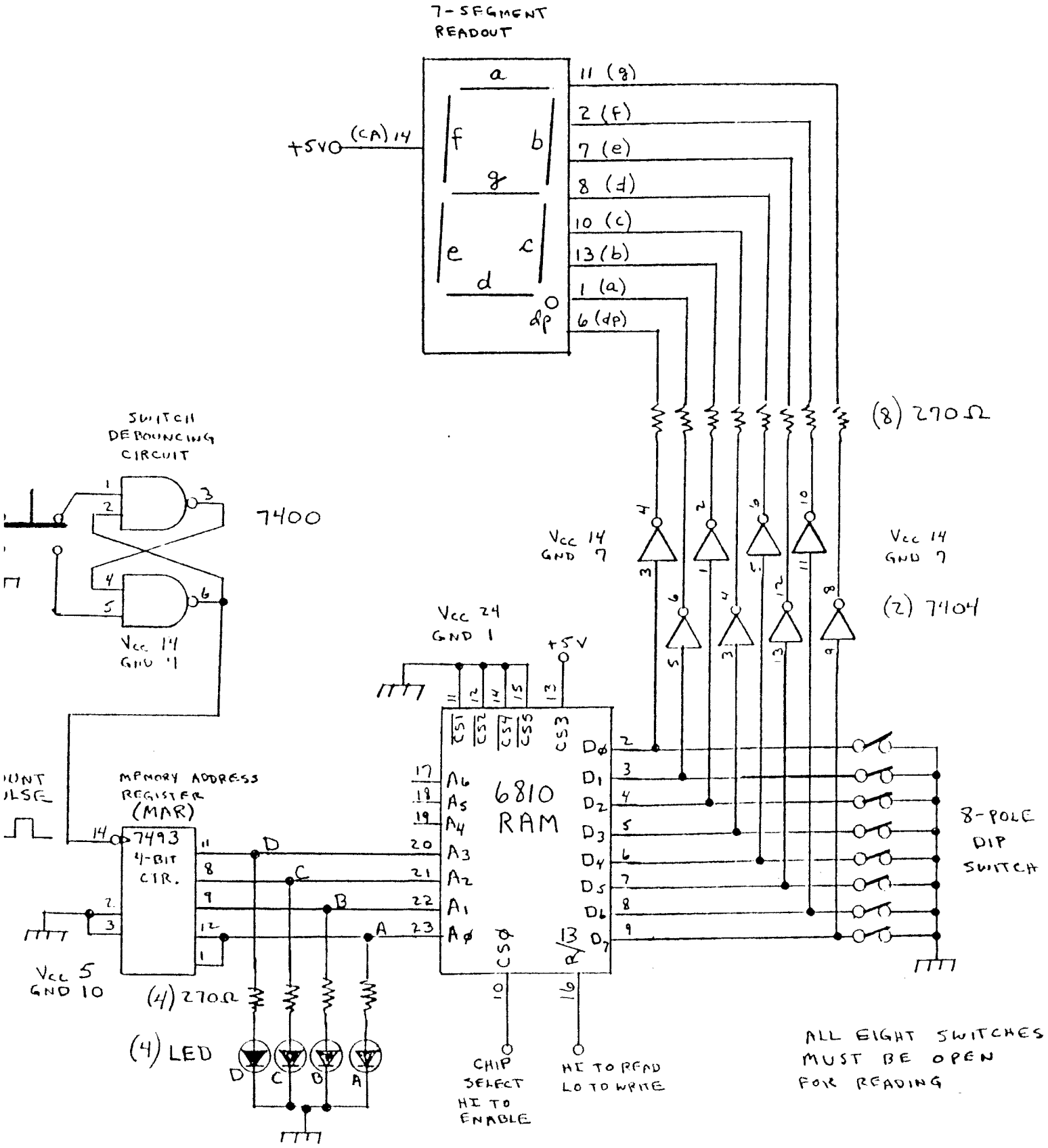

+5V
200mA
500Ω
TO-92 (2x)
SQUARE WAVE
GENERATOR @ 100Hz
5V
TENS
DISPLAY
UNITS
DISPLAY
ANODE
ANODE
a b c d e f g
270Ω
(7x)
74157
2-IN x 4-BIT
MUX
SELECT
(1)
A_T (2)
B_T (5)
C_T (11)
D_T (14)
1A
2A
3A
4A
A_U (3)
B_U (6)
C_U (10)
D_U (13)
1B
2B
3B
4B
E
(15)
1Y (4)
2Y (7)
3Y (9)
4Y (12)
7447
DECODER
(7) A
(1) B
(2) C
(6) D
a
b
c
d
e
f
g
7490
TENS DECADE
(SOURCE A)
7490
UNITS DECADE
(SOURCE B)
D_T CK
C_T
B_T
A_T
D_U
C_U CK
B_U
A_U
COUNT PULSES
(MANUAL)

ProDev, Inc. All Rights Reserved DATE: Apr 2nd, 1992	TITLE: 4 by 1 Static RAM DRAWN BY: CK DESIGNED BY: Chuck Kelly CHECK BY:



Tri-State Buffer

READING AND WRITING WITH A RAM



Writing into the RAM

Start with the CS0 (chip select) line held LO, connected to the ground bus. This disables the RAM prior to addressing it.

Bring the R/$\overline{W}$ line LO by connecting it to the ground bus. This sets up the RAM for the WRITE mode.

For each byte to be written, repeat the following procedure:

1. Step the 4-bit counter (the MAR) and visually verify the address.

2. Switch the desired byte onto the bidirectional data bus.

3. Momentarily bring the CS0 line HI by touching it to the +5V bus; this momentarily enables, or selects, the RAM. Then return CS0 to LO by reconnecting it to the ground bus.

Reading out of the RAM

Start with the CS0 line held LO, connected to the ground bus.

Open all the dip switches. Better yet, completely remove the dip switch package from the board so that there can be no data line held LO by a switch closure to ground.

Bring the R/$\overline{W}$ line HI by connecting it to the +5V bus. This sets up the RAM for the READ mode.

Bring the CS0 line HI by connecting it to the +5V bus. This enables the RAM in the READ mode.

Step the 4-bit counter through all its states. The count pulses can be delivered manually or by a sig gen operating at low frequency.