Kansas Fest 93

Session: Digital Electronics

Presenter: Chuck Kelly / ProDev, Inc.
Basic Electronics Review

It may help in your understanding of electricity if you compare it to fluid flowing in pipes.

<table>
<thead>
<tr>
<th>Electricity</th>
<th>Fluid</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage</td>
<td>PSI pressure in a water pipe.</td>
</tr>
<tr>
<td>Current</td>
<td>Flow rate (Gallons Per Minute)</td>
</tr>
<tr>
<td>Resistance</td>
<td>Flow restrictor</td>
</tr>
</tbody>
</table>

Ohm's Law: \[ E = \frac{V}{I} \]

Voltage - Force that is being exerted on the electrons
Symbol: "E" or "V"
Unit: "volt"

Current - Flow rate of the electrons.
Symbol: "I"
Unit: "Amp"

Resistance - Resistance to the flow of electrons.
Symbol: "Ω"
Unit: "Ohm"

Capacitor - Block the flow of Direct Current and pass the flow of Alternating Current.
Symbol: "F"
Term: "Capacitance"
Unit: "Farad"

Inductor - Block the flow of Alternating Current and pass the flow of Direct Current.
Symbol: "H"
Term: "Inductance"
Unit: "Henry"

Other schematic symbols

Common
Fuse
Connection (old way) (new way)
Ground (old way) (new way)
TTL logic levels

5V
: Logic 1
2V

-----------------------------

: Undefined logic level

-----------------------------

0.8V
: Logic 0
0.0V

Binary, Hex, BCD

<table>
<thead>
<tr>
<th>Decimal</th>
<th>Binary</th>
<th>BCD</th>
<th>Hex</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0000</td>
<td>0000</td>
<td>00</td>
</tr>
<tr>
<td>1</td>
<td>0001</td>
<td>0001</td>
<td>01</td>
</tr>
<tr>
<td>2</td>
<td>0010</td>
<td>0010</td>
<td>02</td>
</tr>
<tr>
<td>3</td>
<td>0011</td>
<td>0011</td>
<td>03</td>
</tr>
<tr>
<td>4</td>
<td>0100</td>
<td>0100</td>
<td>04</td>
</tr>
<tr>
<td>5</td>
<td>0101</td>
<td>0101</td>
<td>05</td>
</tr>
<tr>
<td>6</td>
<td>0110</td>
<td>0110</td>
<td>06</td>
</tr>
<tr>
<td>7</td>
<td>0111</td>
<td>0111</td>
<td>07</td>
</tr>
<tr>
<td>8</td>
<td>1000</td>
<td>1000</td>
<td>08</td>
</tr>
<tr>
<td>9</td>
<td>1001</td>
<td>1001</td>
<td>09</td>
</tr>
<tr>
<td>10</td>
<td>1010</td>
<td>0001 0000</td>
<td>0A</td>
</tr>
<tr>
<td>11</td>
<td>1011</td>
<td>0001 0001</td>
<td>0B</td>
</tr>
<tr>
<td>12</td>
<td>1100</td>
<td>0001 0010</td>
<td>0C</td>
</tr>
<tr>
<td>13</td>
<td>1101</td>
<td>0001 0011</td>
<td>0D</td>
</tr>
<tr>
<td>14</td>
<td>1110</td>
<td>0001 0100</td>
<td>0E</td>
</tr>
<tr>
<td>15</td>
<td>1111</td>
<td>0001 0101</td>
<td>0F</td>
</tr>
<tr>
<td>16</td>
<td>10000</td>
<td>0001 0110</td>
<td>10</td>
</tr>
</tbody>
</table>

ASCII

<table>
<thead>
<tr>
<th>Character</th>
<th>ASCII code (Hex)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>41</td>
</tr>
<tr>
<td>B</td>
<td>42</td>
</tr>
<tr>
<td>Z</td>
<td>5A</td>
</tr>
</tbody>
</table>
GATES

BUFFERS

\[ A \rightarrow x \]

1 IN 1 OUT

\( x = A \)

INVERTERS

\[ A \rightarrow x \]

0 IN 1 OUT

\( x = \overline{A} \)

AND

\[ \begin{array}{|c|c|c|}
\hline
A & B & x = A \cdot B \\
\hline
0 & 0 & 0 \\
0 & 1 & 0 \\
1 & 0 & 0 \\
1 & 1 & 1 \\
\hline
\end{array} \]

NAND

\[ x = \overline{A \cdot B} \]

OR

\[ \begin{array}{|c|c|c|}
\hline
A & B & x = A + B \\
\hline
0 & 0 & 0 \\
0 & 1 & 1 \\
1 & 0 & 1 \\
1 & 1 & 1 \\
\hline
\end{array} \]

NOR

\[ x = \overline{A + B} \]

Booleans

\[ x = A \cdot B \cdot C \]

\[ x = A \cdot B \cdot C \]

\[ x = A + B + C \]

\[ x = A + B + C \]
**Boolean Theorems**

\[
\begin{align*}
X \cdot 0 &= 0 & \bar{X} + \bar{X} &= X \\
X \cdot 1 &= X & X + 1 &= 1 \\
X \cdot X &= X & X + X &= X \\
X \cdot \bar{X} &= 0 & X + \bar{X} &= 1 \\
X + Y &= Y + X \\
X \cdot Y &= Y \cdot X \\
x + (y + z) &= (x + y) + z = x + y + z \\
x(yz) &= (xy)z = xyz \\
x(y + z) &= xy + xz \\
(w + x)(y + z) &= wy + xy + wz + xz \\
x + xy &= x \\
x + \bar{x}y &= x + y
\end{align*}
\]

**De Morgan's Theorems**

\[
\begin{align*}
\bar{X} + \bar{Y} &= \bar{X} \cdot \bar{Y} \\
\bar{X} + Y &= \bar{X} \cdot Y \\
X + Y &= \bar{X} \cdot \bar{Y}
\end{align*}
\]

[Diagram of logic gates]
**Boolean Algebra Examples**

**#1**

\[ A + BC + ABC \]

Demorgans

\[ A \overline{BC} + ABC \]

Factor out common BC

\[ BC (\overline{A} + A) \]

\[ X + \overline{X} = 1 \]

\[ BC (1) \]

\[ X \cdot 1 = X \]

\[ BC \]

**#2**

\[(A + BC)(A + B)\]

\[ A \overline{AC} + A \overline{B} + ABC + B \overline{BC} \]

\[ AC + (A \overline{B} + ABC) + 0 \]

\[ AC + A (B + BC) \]

\[ AC + A (B + C) \]

\[ AC + AB + BC \]

\[ AC + AB \]

**#3**

\[ \overline{A} + \overline{B} + \overline{C} + \overline{ABC} + ABC \]

\[ A \overline{BC} + \overline{B} \overline{C} + ABC \]

\[ \overline{B} \overline{C} + (ABC + \overline{ABC}) \]

\[ \overline{A} \overline{B} \overline{C} + 1 \]

\[ 1 \]

**#4**

\[ (A + B \cdot \overline{B + C}) \cdot (\overline{B} \overline{C} + \overline{CD}) \]

\[ (A + B + C)(B + C) \]

\[ ABCD + B C D + B C \overline{C} \]

\[ ABCD + (B C D + B CD) \]

\[ ABCD + B CD \]

\[ BCD (A + 1) \]

\[ BCD \]
**Flip-Flops**

**SR Latch**

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td><strong>NO CHANGE</strong></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td><strong>Q = 1</strong></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td><strong>Q = 0</strong></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td><strong>INVALID</strong></td>
</tr>
</tbody>
</table>

**D Latch**

<table>
<thead>
<tr>
<th>E</th>
<th>D</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td><strong>X</strong></td>
<td>Q₀</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**D Flip-Flop (D-F-F)**

<table>
<thead>
<tr>
<th>D CLK</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**JK Flip-Flop (JK-F-F)**

<table>
<thead>
<tr>
<th>J</th>
<th>K</th>
<th>CLK</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td><strong>Q₀</strong></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td><strong>Q₀</strong></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td><strong>Q₀</strong></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td><strong>Q₀ (Toggles)</strong></td>
</tr>
</tbody>
</table>

**Set & Clear**

<table>
<thead>
<tr>
<th>SET</th>
<th>CLR</th>
<th>RESPONSE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td><strong>NORMAL OPERATION</strong></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Q = 1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Q = 0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td><strong>NOT USED</strong></td>
</tr>
</tbody>
</table>

*Asynchronous Set & Clear*
FOUR BIT SHIFT REGISTER

DATA IN

SHIFT PULSES

SHIFT PULSES

DATA IN

Q1

Q2

Q3

Q4
Clock pulses

Flip-flops wired as a 3-bit binary ripple counter (MOD-8).

<table>
<thead>
<tr>
<th>2</th>
<th>1</th>
<th>0</th>
<th>Clock pulse</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>5</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>6</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>7</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>8</td>
</tr>
</tbody>
</table>
BCD to 7-segment decoder/driver

- BCD input: D, C, B, A
- Cathode connections: a, b, c, d, e, f, g
- Anode connections: A, B, C, D

### 7446 or 7447

For current limiting

### 7447A

- VCC 16
- GND 8

### MAN-72

- ANODE (1)
- CATHODE-a
- CATHODE-f
- CATHODE-c
- CATHODE-g
- CATHODE-d
- N.C. (2)

### NOTES

1. Redundant anodes
2. Leave pin unconnected
Writing into the RAM

Start with the CS0 (chip select) line held LO, connected to the ground bus. This disables the RAM prior to addressing it.

Bring the R/W line LO by connecting it to the ground bus. This sets up the RAM for the WRITE mode.

For each byte to be written, repeat the following procedure:

1. Step the 4-bit counter (the MAR) and visually verify the address.
2. Switch the desired byte onto the bidirectional data bus.
3. Momentarily bring the CS0 line HI by touching it to the +5V bus; this momentarily enables, or selects, the RAM. Then return CS0 to LO by reconnecting it to the ground bus.

Reading out of the RAM

Start with the CS0 line held LO, connected to the ground bus.

Open all the dip switches. Better yet, completely remove the dip switch package from the board so that there can be no data line held LO by a switch closure to ground.

Bring the R/W line HI by connecting it to the +5V bus. This sets up the RAM for the READ mode.

Bring the CS0 line HI by connecting it to the +5V bus. This enables the RAM in the READ mode.

Step the 4-bit counter through all its states. The count pulses can be delivered manually or by a sig gen operating at low frequency.