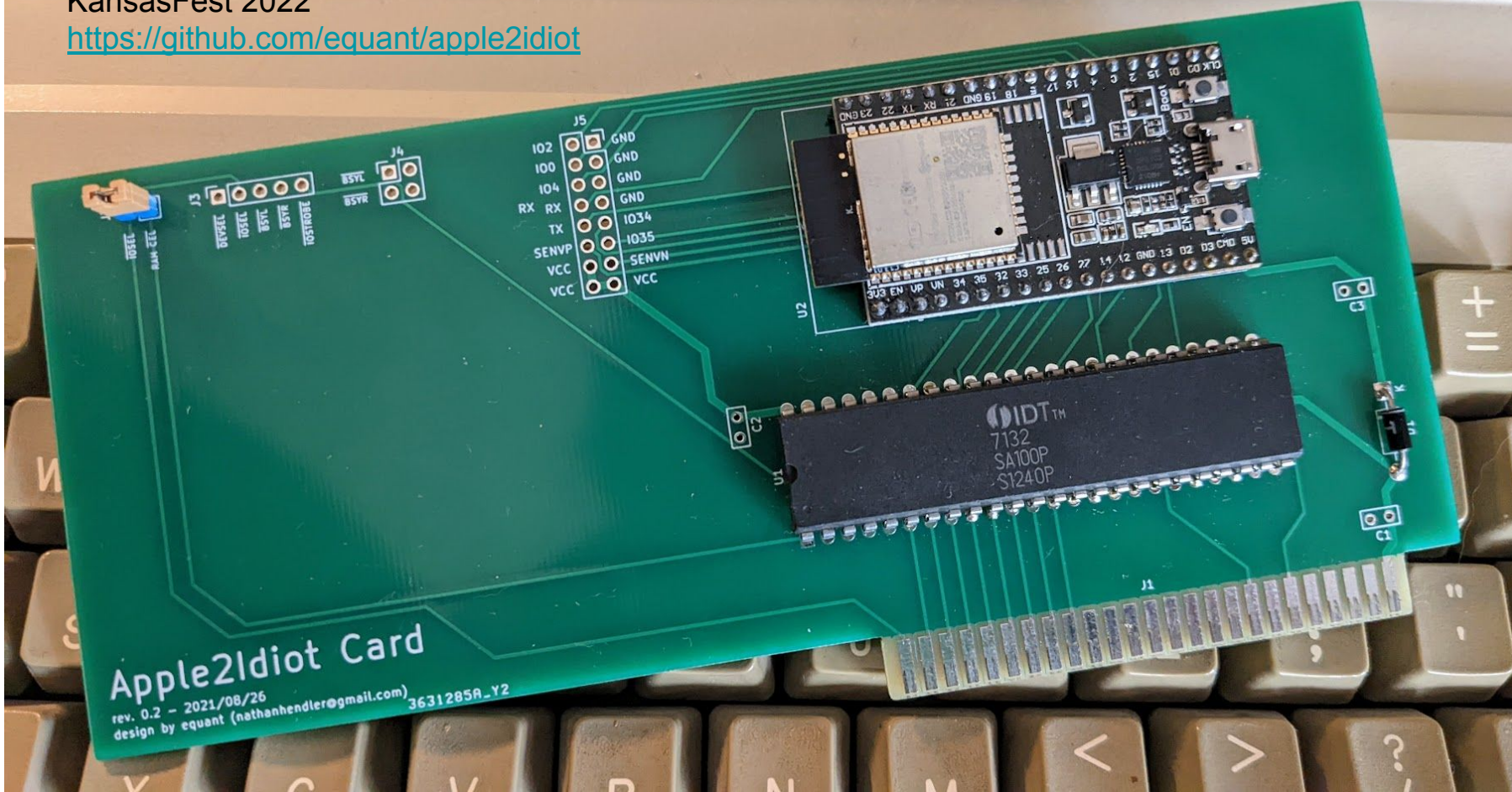


KansasFest 2022

<https://github.com/equant/apple2idiot>



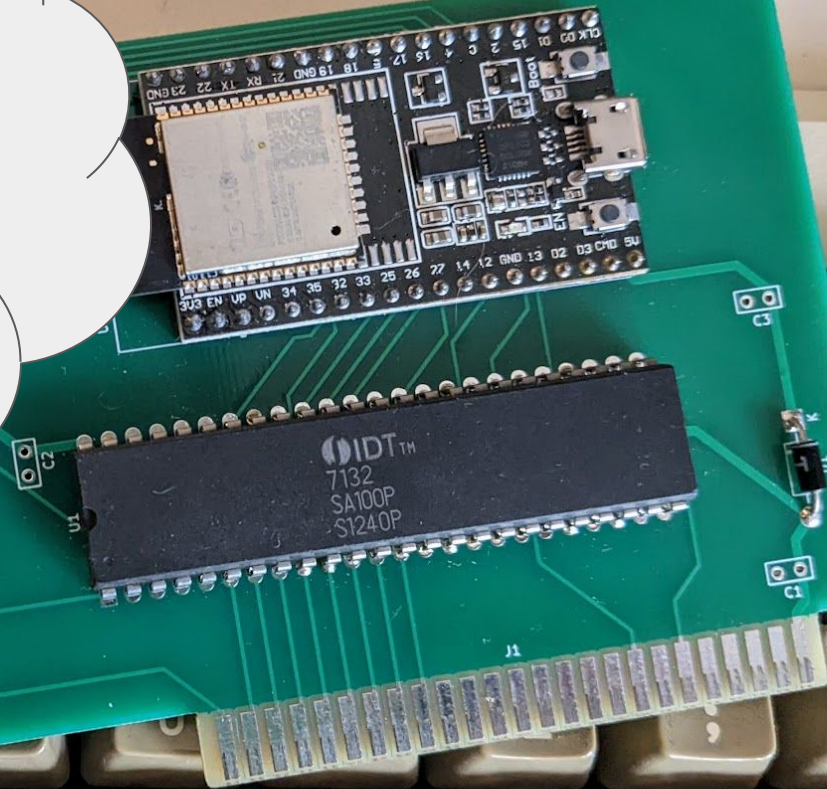
An expansion card that provides an interface to ESP32 microcontroller via dual-port ram.

ESP32: 240 MHz Micro with Wifi / Bluetooth / ADC

Apple2Idiot Card

rev. 0.2 - 2021/08/26
design by equant (nathanhender@gmail.com)

3631285A_Y2



About me / Full disclosure

- Macintosh 68k System 6/7 background
 - Grackle 68k
 - mpd client
 - Robotfindskitten port for Mayan Apocalypse Edition
 - RetroBridgeBBS
- Started Apple II stuff with this project.
 - I mostly don't know what I'm doing
 - I couldn't have done any of this without the Apple II community.

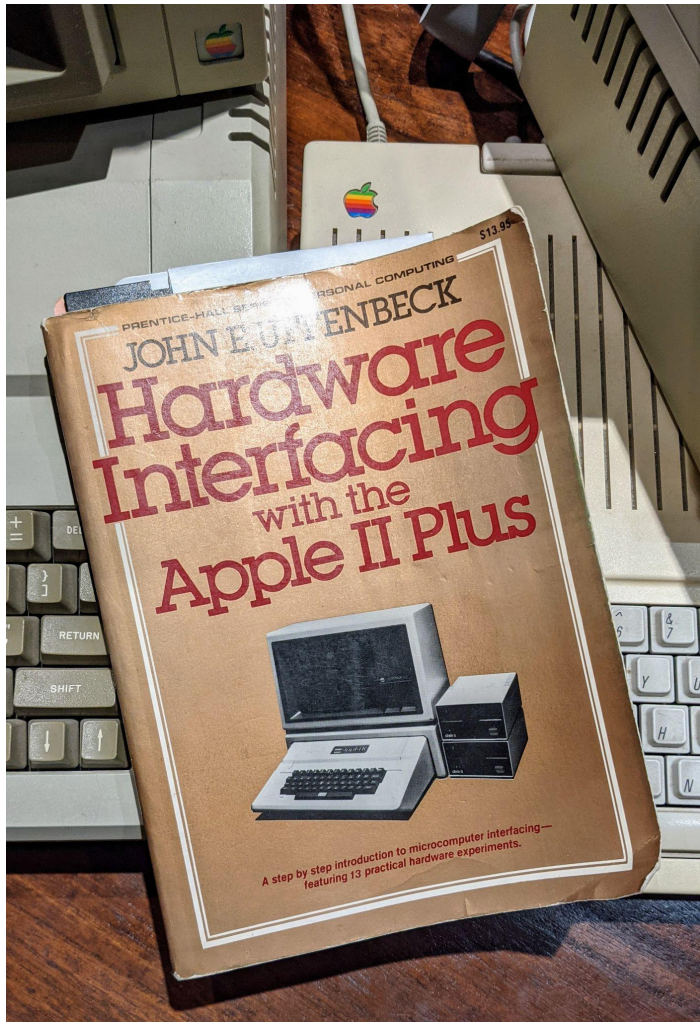
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*Proof I don't
know what I'm
doing*

```
␣10 WIFICONNECT=10
␣RUN
?SYNTAX ERROR IN 10
␣LIST

10 W IF IC ON NECT = 10
```

Hardware Interfacing with the Apple II Plus

Are you tired of game playing on your Apple computer?

Are you bored running other peoples' canned software?

Well, in this book, **John Uffenbeck** shows you how to accomplish such projects as programming your Apple to turn on a room light, your furnace, or your air conditioner; or to display the exponential charging curve of voltage on a capacitor; or the temperature versus time of day.

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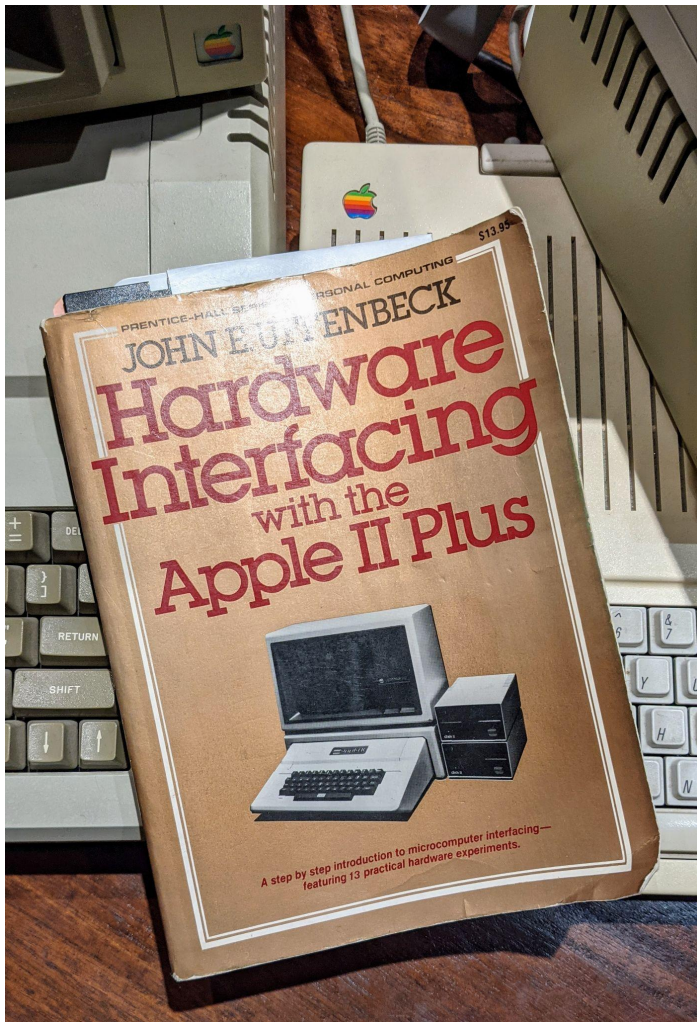


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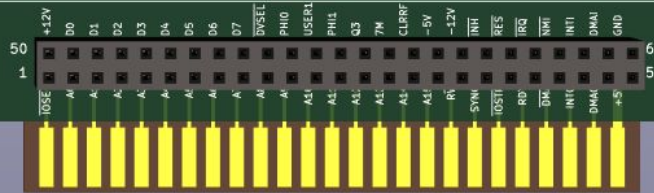
Project Priorities

- Develop hardware
- Custom PCB
- Easy
- Hand solderable
 - Through-hole components
 - Low component count
- Do something neat

JLCLJLCLJL

Apple II Breadboard Adapter

rev. 1.1 - 2021/02/08
design by Renee Harke



<https://github.com/rharke/apple-ii-breadboard-card>

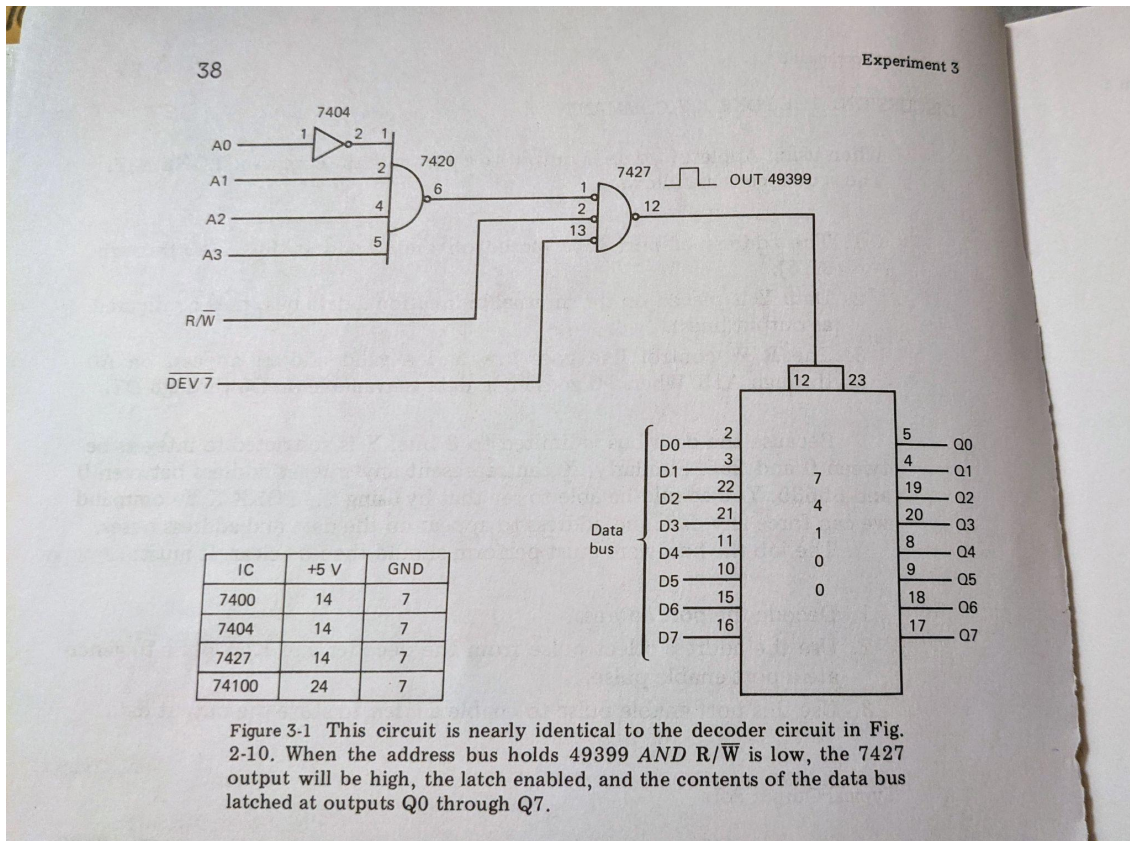
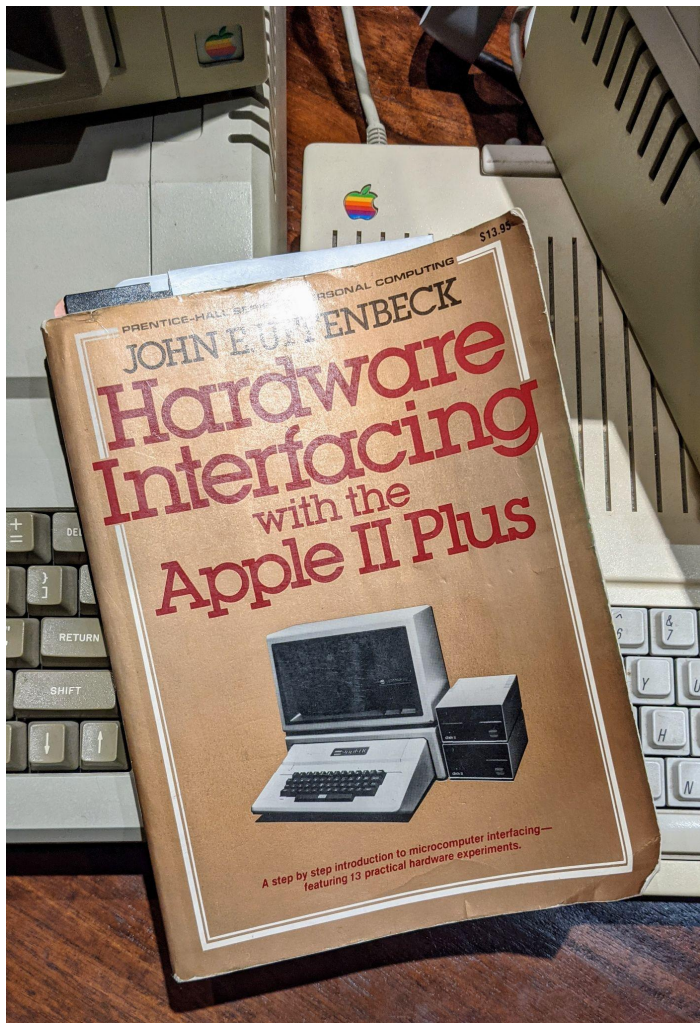


Figure 3-1 This circuit is nearly identical to the decoder circuit in Fig. 2-10. When the address bus holds 49399 AND R/\bar{W} is low, the 7427 output will be high, the latch enabled, and the contents of the data bus latched at outputs Q0 through Q7.

Stuff in yellow comes from Apple II
(via card edge)

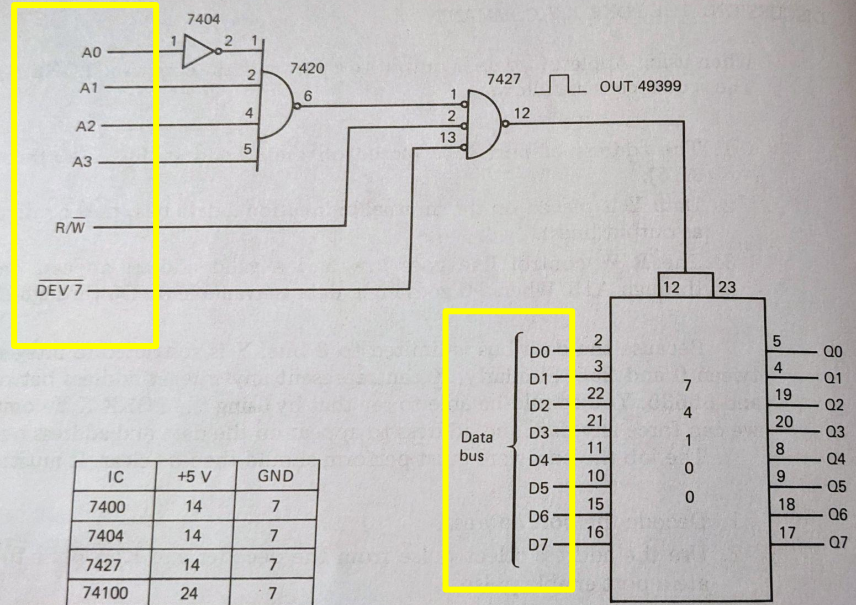


Figure 3-1 This circuit is nearly identical to the decoder circuit in Fig. 2-10. When the address bus holds 49399 AND R/\bar{W} is low, the 7427 output will be high, the latch enabled, and the contents of the data bus latched at outputs Q0 through Q7.

Stuff in yellow comes from Apple II
(via card edge)

Only 4 LSB from Address
Bus



All 8 Bits from Data

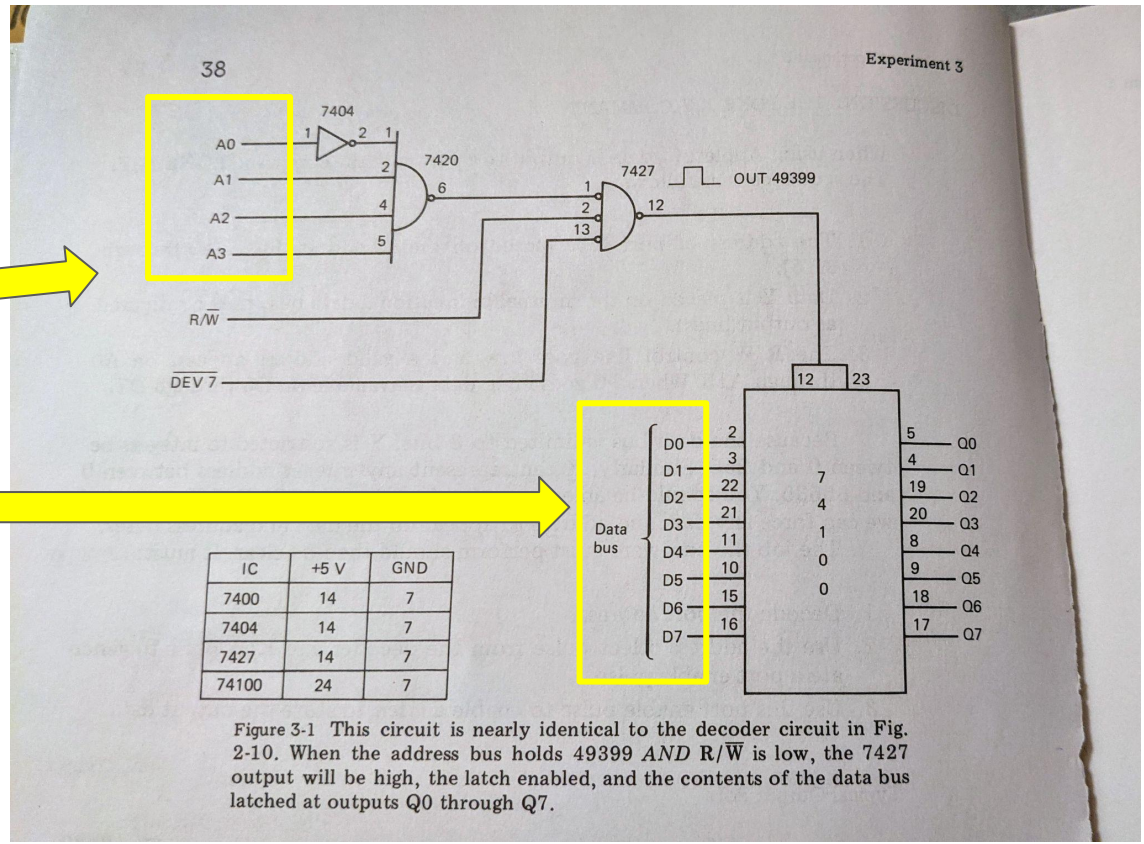


Figure 3-1 This circuit is nearly identical to the decoder circuit in Fig. 2-10. When the address bus holds 49399 AND R/\bar{W} is low, the 7427 output will be high, the latch enabled, and the contents of the data bus latched at outputs Q0 through Q7.

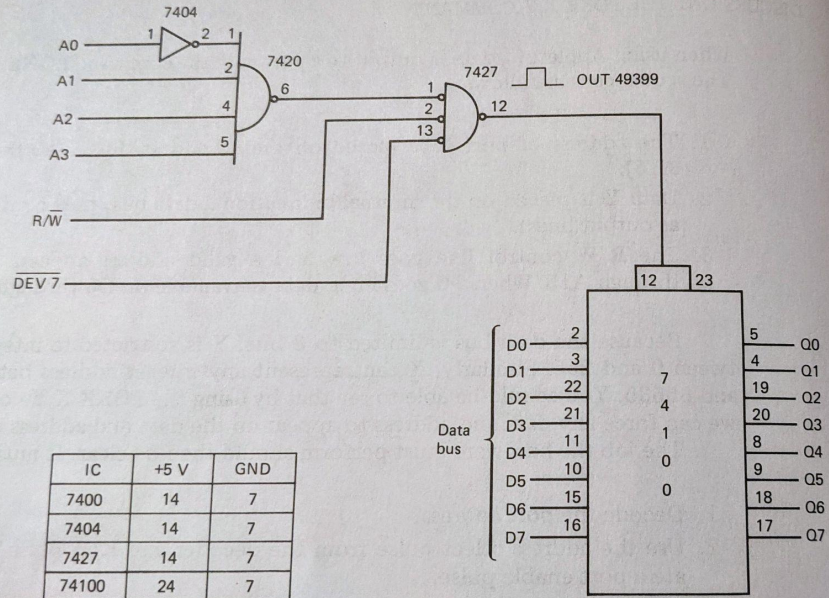


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Low when card is "selected"

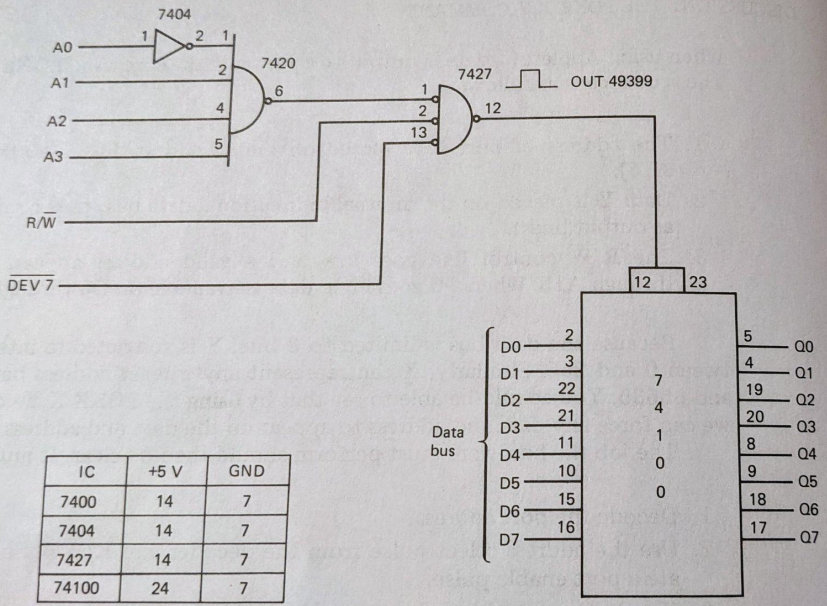
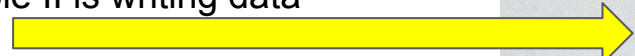


Figure 3-1 This circuit is nearly identical to the decoder circuit in Fig. 2-10. When the address bus holds 49399 AND R/\bar{W} is low, the 7427 output will be high, the latch enabled, and the contents of the data bus latched at outputs Q0 through Q7.

Low when Apple II is writing data



Low when card is "selected"



499399 == 0b1100000011110111
`POKE 499399, 42`

And Apple II is writing data

When low card is "selected"

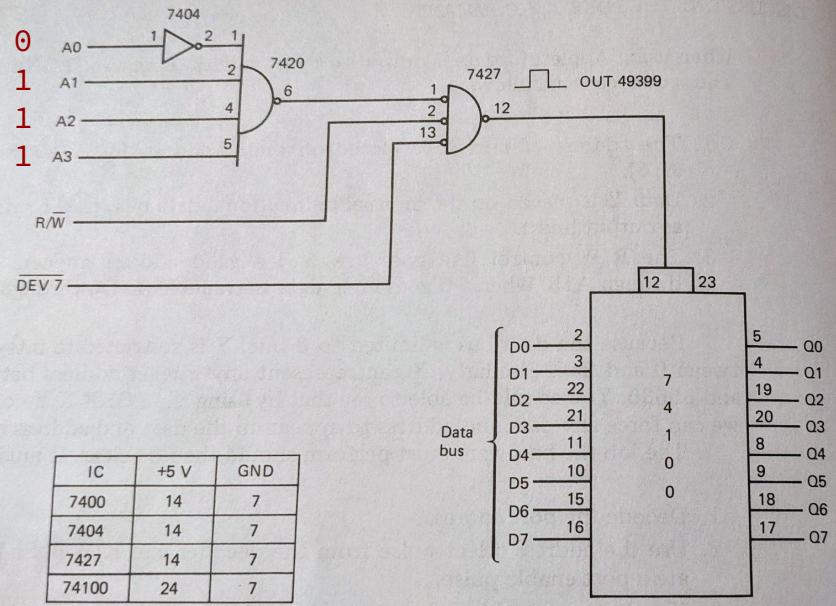
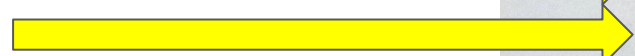
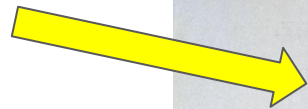


Figure 3-1 This circuit is nearly identical to the decoder circuit in Fig. 2-10. When the address bus holds 49399 AND R/W is low, the 7427 output will be high, the latch enabled, and the contents of the data bus latched at outputs Q0 through Q7.

CARD #1

~~DENSEL~~ DENSEL

D0
D1
D2
D3
D4
D5
D6
D7

R/W

A0
A1
A2
A3

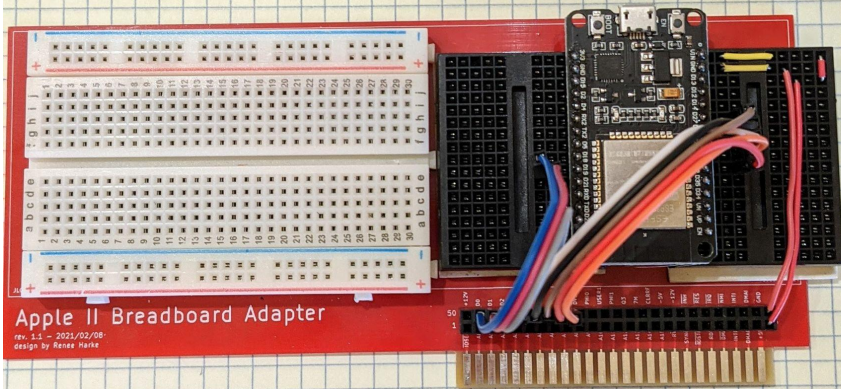
ESP32 PINS

~~D0~~ ~~D1~~ ~~D2~~ ~~D3~~ D35 input only

D18
D19
D23
D25
D26
D27
D32
D33

D34 input only

~~D4~~ D4
~~D5~~ D5
~~D13~~ D13
~~D14~~ D14



CARD #1

~~D0-D7~~ DEVSSEL

D0
D1
D2
D3
D4
D5
D6
D7

R/W

A0
A1
A2
A3

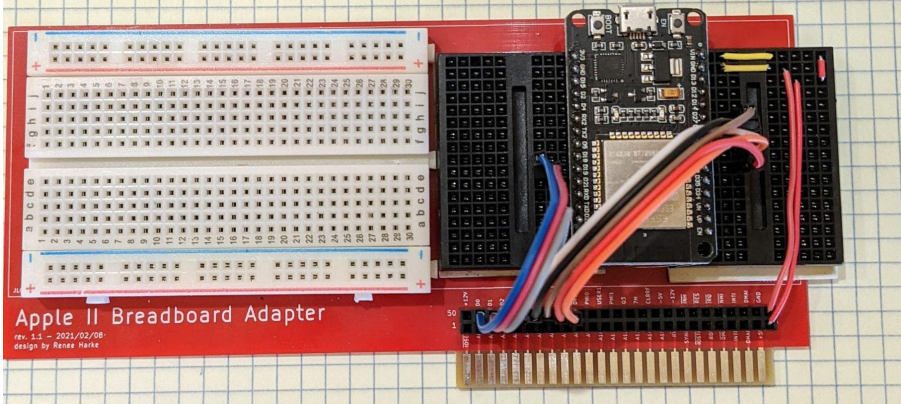
ESP32 PINS

~~D8-D14~~ D35 input only

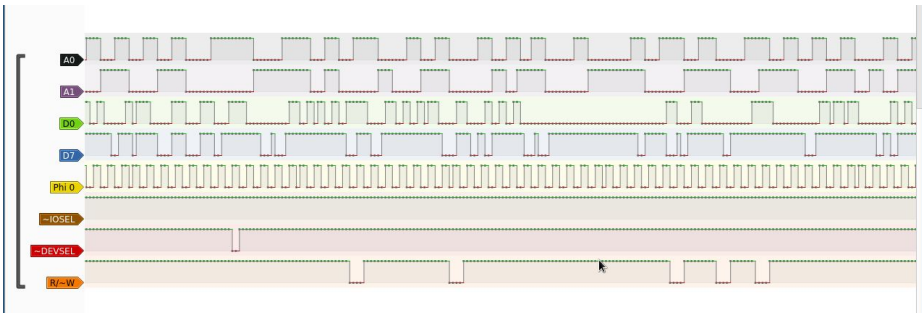
D18
D19
D23
D25
D26
D27
D32
D33

D34 input only

~~D4~~ D4
~~D5~~ D5
~~D13~~ D13
~~D14~~ D14

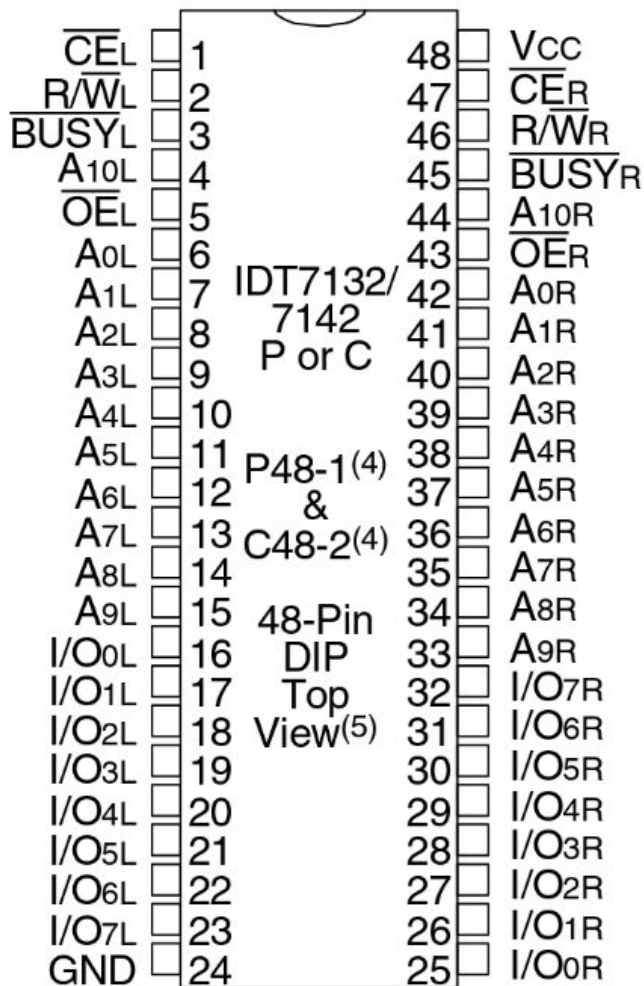


Didn't work. ~2us interrupt latency



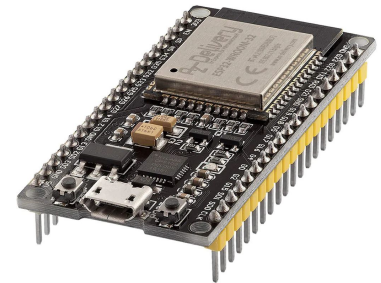
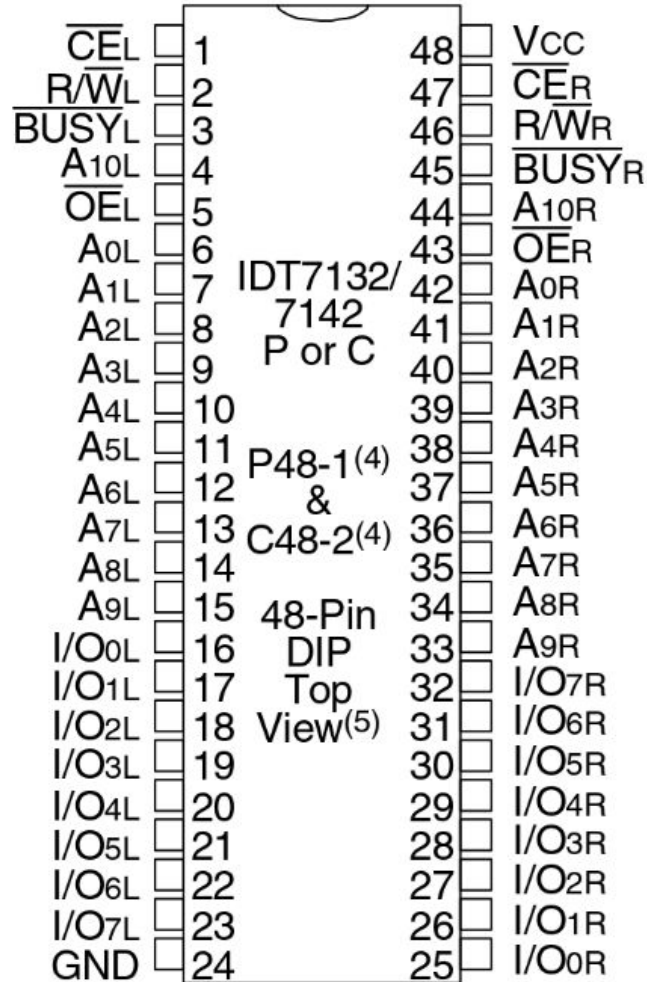
IDT7132

HIGH SPEED
2K x 8 DUAL PORT
STATIC RAM



IDT7132

HIGH SPEED
2K x 8 DUAL PORT
STATIC RAM

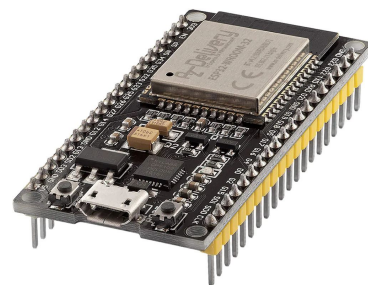


IDT7132

HIGH SPEED
2K x 8 DUAL PORT
STATIC RAM



$\overline{\text{CEL}}$	1		48	VCC
R/WL	2		47	$\overline{\text{CER}}$
BUSYL	3		46	R/WR
$\text{A}_{10\text{L}}$	4		45	$\overline{\text{BUSYR}}$
$\overline{\text{OEL}}$	5		44	$\text{A}_{10\text{R}}$
$\text{A}_{0\text{L}}$	6	IDT7132/ 7142 P or C	43	$\overline{\text{OER}}$
$\text{A}_{1\text{L}}$	7		42	$\text{A}_{0\text{R}}$
$\text{A}_{2\text{L}}$	8		41	$\text{A}_{1\text{R}}$
$\text{A}_{3\text{L}}$	9		40	$\text{A}_{2\text{R}}$
$\text{A}_{4\text{L}}$	10		39	$\text{A}_{3\text{R}}$
$\text{A}_{5\text{L}}$	11		38	$\text{A}_{4\text{R}}$
$\text{A}_{6\text{L}}$	12		37	$\text{A}_{5\text{R}}$
$\text{A}_{7\text{L}}$	13		36	$\text{A}_{6\text{R}}$
$\text{A}_{8\text{L}}$	14		35	$\text{A}_{7\text{R}}$
$\text{A}_{9\text{L}}$	15		34	$\text{A}_{8\text{R}}$
$\text{I/O}_{0\text{L}}$	16		33	$\text{A}_{9\text{R}}$
$\text{I/O}_{1\text{L}}$	17		32	$\text{I/O}_{7\text{R}}$
$\text{I/O}_{2\text{L}}$	18		31	$\text{I/O}_{6\text{R}}$
$\text{I/O}_{3\text{L}}$	19	30	$\text{I/O}_{5\text{R}}$	
$\text{I/O}_{4\text{L}}$	20	29	$\text{I/O}_{4\text{R}}$	
$\text{I/O}_{5\text{L}}$	21	28	$\text{I/O}_{3\text{R}}$	
$\text{I/O}_{6\text{L}}$	22	27	$\text{I/O}_{2\text{R}}$	
$\text{I/O}_{7\text{L}}$	23	26	$\text{I/O}_{1\text{R}}$	
GND	24	25	$\text{I/O}_{0\text{R}}$	

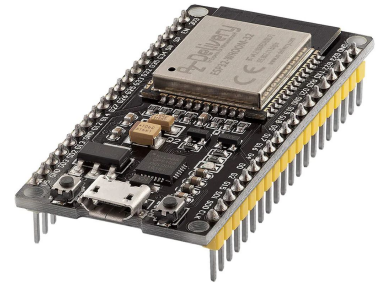
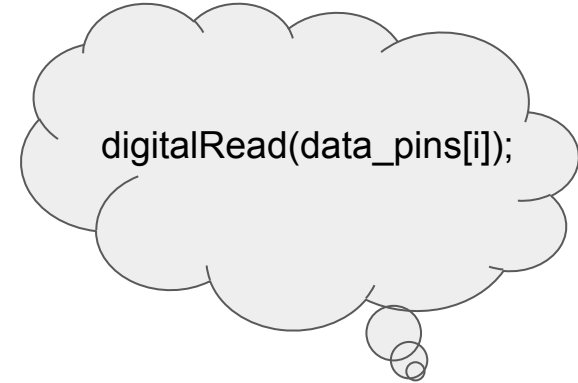


IDT7132

HIGH SPEED
2K x 8 DUAL PORT
STATIC RAM



$\overline{CE_L}$	1		48	V_{CC}
R/WL	2		47	$\overline{CE_R}$
BUSYL	3		46	R/W _R
A _{10L}	4		45	$\overline{BUSY_R}$
$\overline{OE_L}$	5		44	A _{10R}
A _{0L}	6	IDT7132/	43	$\overline{OE_R}$
A _{1L}	7	7142	42	A _{0R}
A _{2L}	8	P or C	41	A _{1R}
A _{3L}	9		40	A _{2R}
A _{4L}	10		39	A _{3R}
A _{5L}	11	P48-1(4)	38	A _{4R}
A _{6L}	12	&	37	A _{5R}
A _{7L}	13	C48-2(4)	36	A _{6R}
A _{8L}	14		35	A _{7R}
A _{9L}	15	48-Pin	34	A _{8R}
I/O _{0L}	16	DIP	33	A _{9R}
I/O _{1L}	17	Top	32	I/O _{7R}
I/O _{2L}	18	View ⁽⁵⁾	31	I/O _{6R}
I/O _{3L}	19		30	I/O _{5R}
I/O _{4L}	20		29	I/O _{4R}
I/O _{5L}	21		28	I/O _{3R}
I/O _{6L}	22		27	I/O _{2R}
I/O _{7L}	23		26	I/O _{1R}
GND	24		25	I/O _{0R}

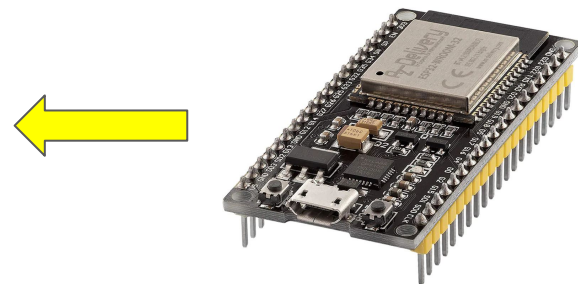
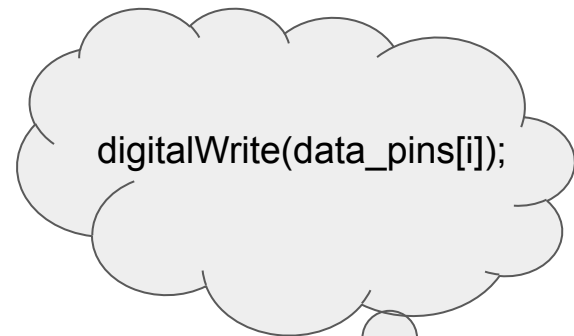


IDT7132

HIGH SPEED
2K x 8 DUAL PORT
STATIC RAM



\overline{CE}_L	1		48	V_{CC}
R/WL	2		47	\overline{CE}_R
BUSYL	3		46	R/W _R
A _{10L}	4		45	\overline{BUSY}_R
\overline{OE}_L	5		44	A _{10R}
A _{0L}	6	IDT7132/	43	\overline{OE}_R
A _{1L}	7	7142	42	A _{0R}
A _{2L}	8	P or C	41	A _{1R}
A _{3L}	9		40	A _{2R}
A _{4L}	10		39	A _{3R}
A _{5L}	11	P48-1(4)	38	A _{4R}
A _{6L}	12	&	37	A _{5R}
A _{7L}	13	C48-2(4)	36	A _{6R}
A _{8L}	14		35	A _{7R}
A _{9L}	15	48-Pin	34	A _{8R}
I/O _{0L}	16	DIP	33	A _{9R}
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I/O _{3L}	19		30	I/O _{5R}
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I/O _{5L}	21		28	I/O _{3R}
I/O _{6L}	22		27	I/O _{2R}
I/O _{7L}	23		26	I/O _{1R}
GND	24		25	I/O _{0R}



IDT7132

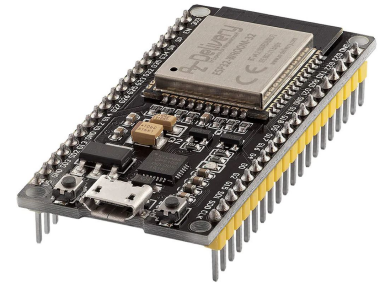
HIGH SPEED
2K x 8 DUAL PORT
STATIC RAM

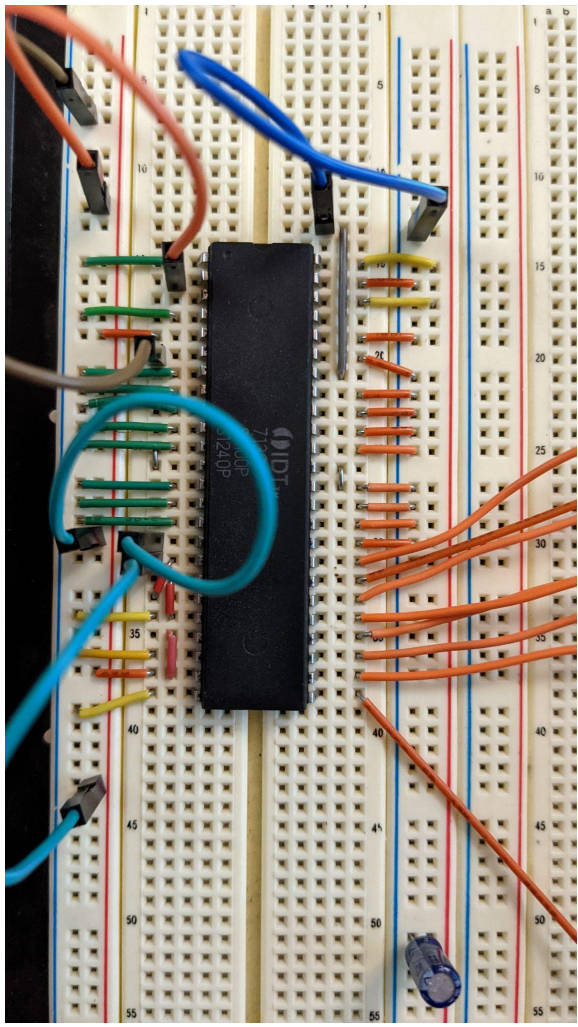
PEEK!

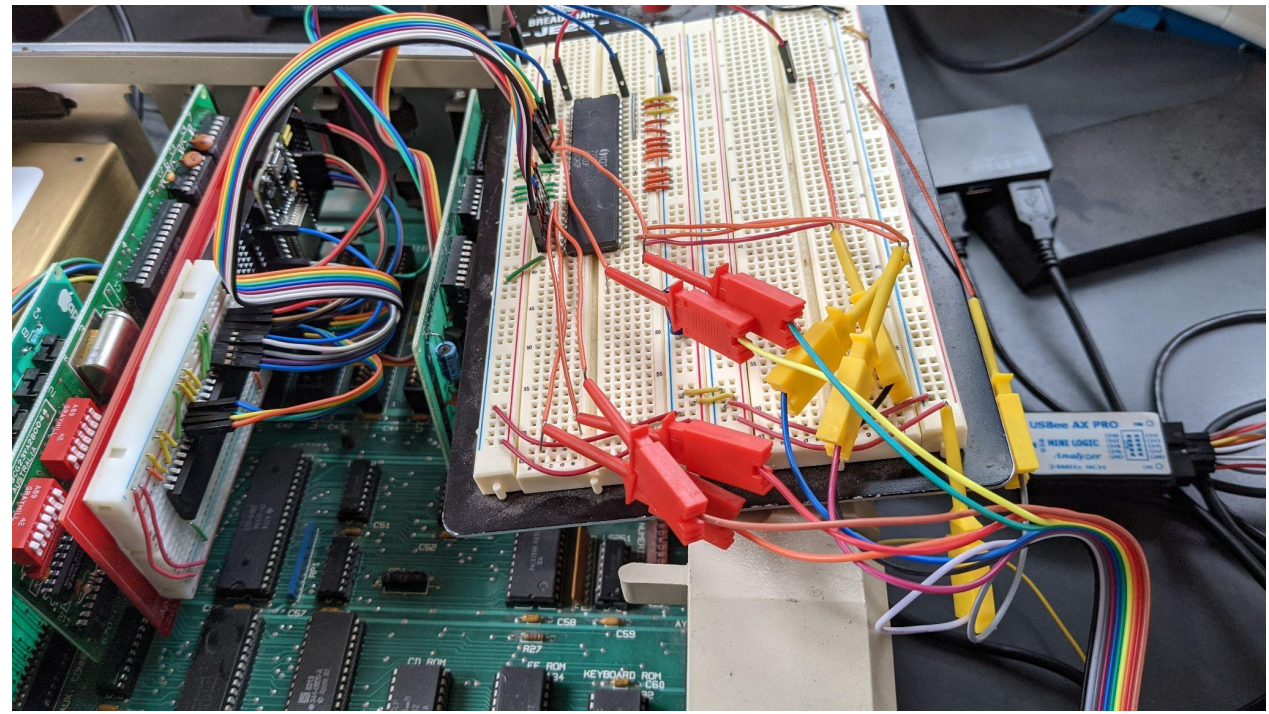
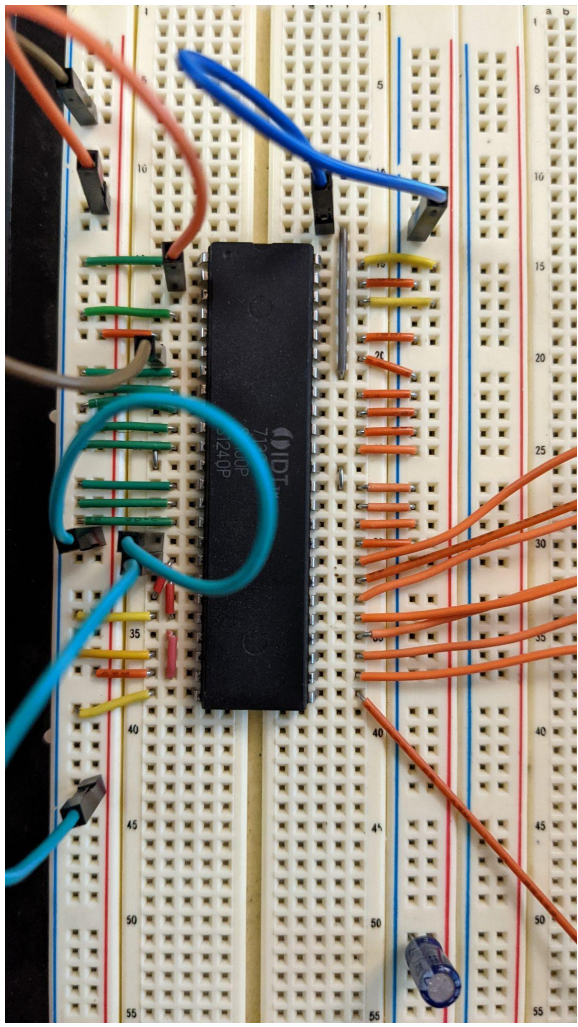


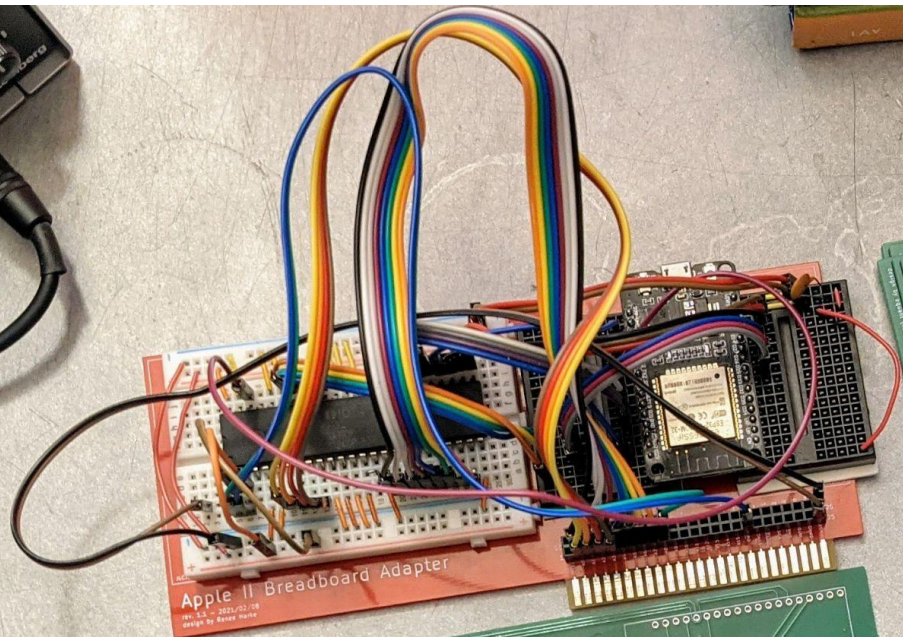
$\overline{\text{CEL}}$	1		48	VCC
R/WL	2		47	$\overline{\text{CER}}$
BUSYL	3		46	R/WR
$\text{A}_{10\text{L}}$	4		45	$\overline{\text{BUSYR}}$
$\overline{\text{OEL}}$	5		44	$\text{A}_{10\text{R}}$
$\text{A}_{0\text{L}}$	6	IDT7132/ 7142 P or C P48-1(4) & C48-2(4) 48-Pin DIP Top View(5)	43	$\overline{\text{OER}}$
$\text{A}_{1\text{L}}$	7		42	$\text{A}_{0\text{R}}$
$\text{A}_{2\text{L}}$	8		41	$\text{A}_{1\text{R}}$
$\text{A}_{3\text{L}}$	9		40	$\text{A}_{2\text{R}}$
$\text{A}_{4\text{L}}$	10		39	$\text{A}_{3\text{R}}$
$\text{A}_{5\text{L}}$	11		38	$\text{A}_{4\text{R}}$
$\text{A}_{6\text{L}}$	12		37	$\text{A}_{5\text{R}}$
$\text{A}_{7\text{L}}$	13		36	$\text{A}_{6\text{R}}$
$\text{A}_{8\text{L}}$	14		35	$\text{A}_{7\text{R}}$
$\text{A}_{9\text{L}}$	15		34	$\text{A}_{8\text{R}}$
$\text{I/O}_{0\text{L}}$	16		33	$\text{A}_{9\text{R}}$
$\text{I/O}_{1\text{L}}$	17		32	$\text{I/O}_{7\text{R}}$
$\text{I/O}_{2\text{L}}$	18		31	$\text{I/O}_{6\text{R}}$
$\text{I/O}_{3\text{L}}$	19	30	$\text{I/O}_{5\text{R}}$	
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$\text{I/O}_{7\text{L}}$	23	26	$\text{I/O}_{1\text{R}}$	
GND	24	25	$\text{I/O}_{0\text{R}}$	

`digitalWrite(data_pins[i]);`

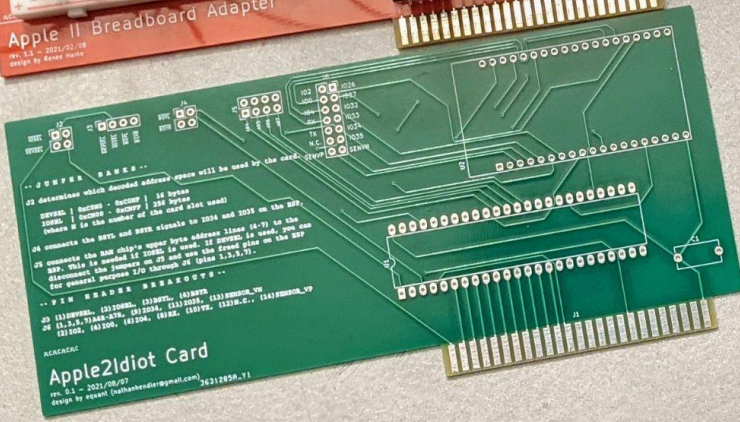




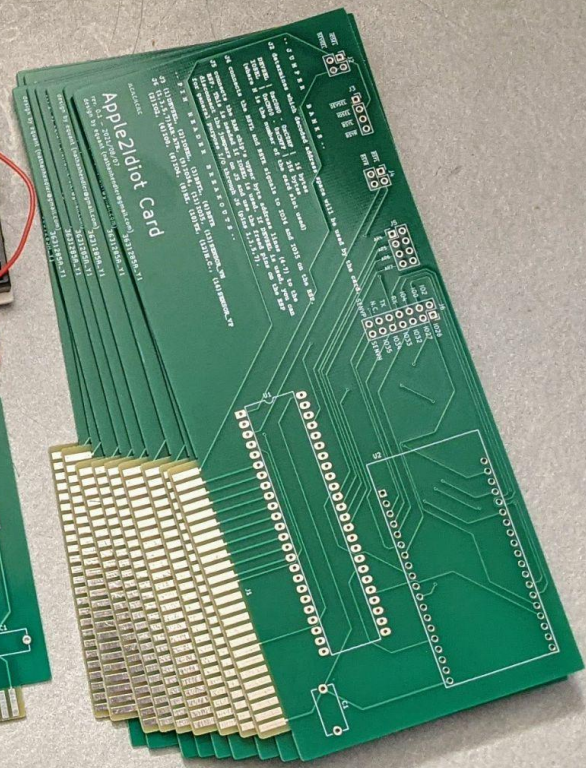




Apple II Breadboard Adapter
rev. 1.1 - 2021/02/08
design by Steve Baker



```
.. J U M P S ..  
03 determine which decoded address space will be used by the card.  
04 connect the 2825 and 2826 signals to 2024 and 2025 on the 287.  
05 connect the 286 chip's upper two address lines (A7-9) to the  
287. 204 is needed if 2024 is used. If 2025 is used, you can  
disconnect the jump on 23 and use the good pin on the 287  
for another purpose. Jig circuitry 05 (pins 1,3,5,7).  
.. P I N H E A D E R ..  
01 1330998.. 1312000.. 1318975.. 1331898.. 1331898.. 1331898.. 1331898.. 1331898.. 1331898..  
02 131312.. 911812.. 911812.. 911812.. 911812.. 911812.. 911812.. 911812.. 911812..  
131312.. 131312.. 131312.. 131312.. 131312.. 131312.. 131312.. 131312.. 131312..  
KICACREK  
Apple2ldiot Card  
rev. 0.1 - 2021/06/07  
design by steve_baker@protonmail.com 36212858-11
```



Apple2ldiot Card

.. JUMPER BANKS ..

J2 determines which decoded address space will be used by the card.
DEVSEL | 0x0000 - 0x00FF | 16 bytes
IOSEL | 0x0100 - 0x01FF | 256 bytes
(where N is the number of the card slot used)

J4 connects the BSYL and BSYR signals to IO34 and IO35 on the ESP.
J5 connects the RAM chip's upper byte address lines (4-7) to the ESP. This is needed if IOSEL is used. If DEVSEL is used, you can disconnect the jumpers on J5 and use the freed pins on the ESP for general purpose I/O through J6 (pins 1,3,5,7).

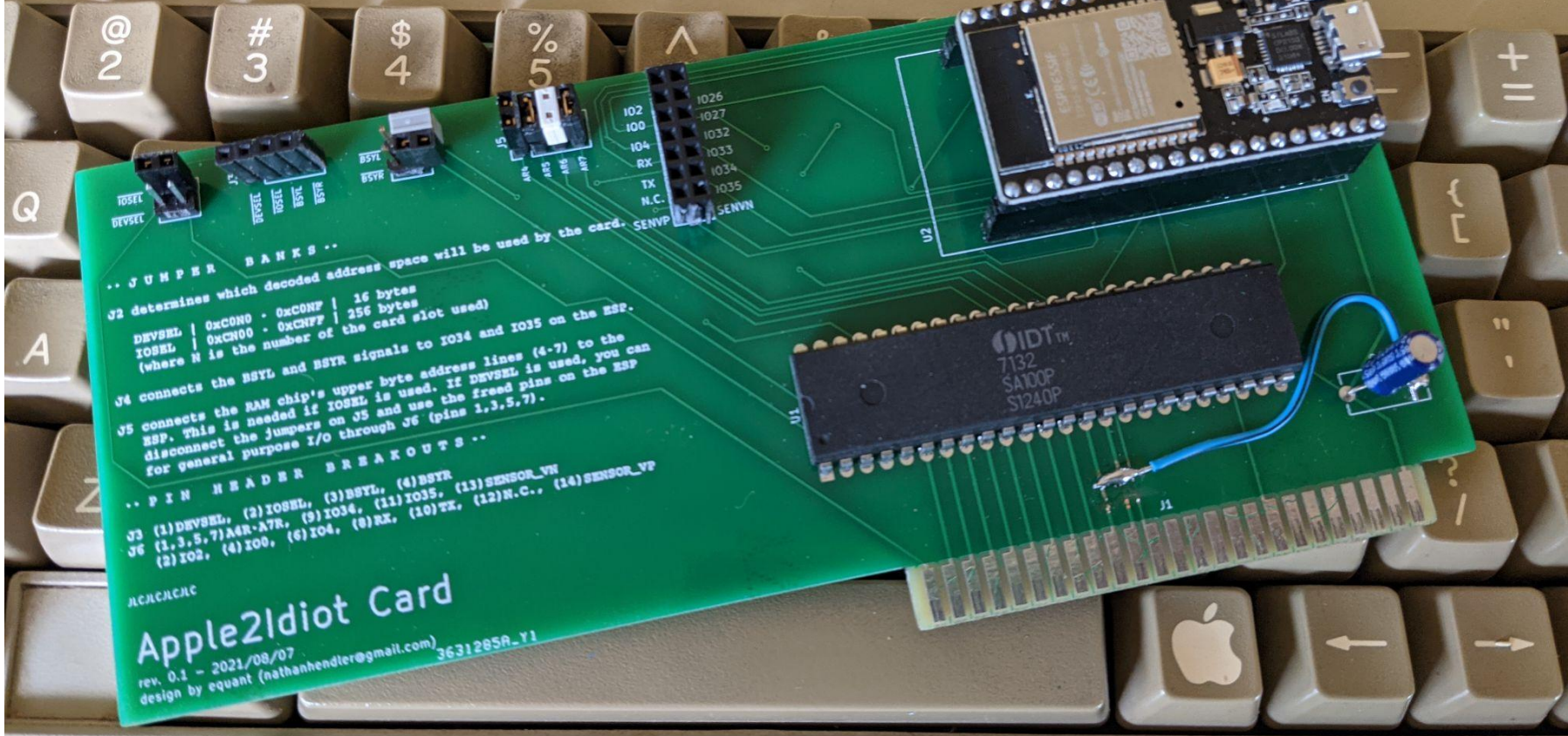
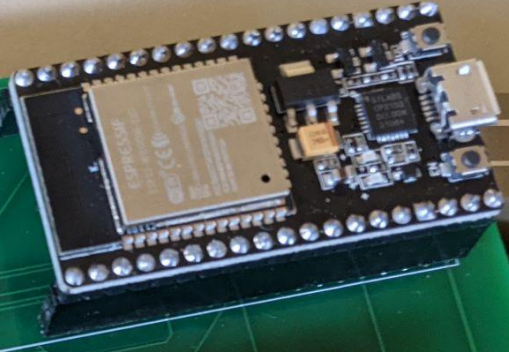
.. PIN HEADER BREAKOUTS ..

J3 (1)DEVSEL, (2)IOSEL, (3)BSYL, (4)BSYR
J6 (1,3,5,7)ADR-ADR, (5)IO34, (11)IO35, (13)SENSOR_VN
(2)IO2, (4)IO0, (6)IO4, (8)RX, (10)TX, (12)N.C., (14)SENSOR_VP

HCCHCJC

Apple2Idiot Card

rev. 0.1 - 2021/08/07
design by equant (nathanhendler@gmail.com) 3631285A-Y1



Apple2Idiot Card

rev. 0.2 - 2021/08/26
design by equant (nathanhender@gmail.com)

3631285A_Y2

- IO2
 - IO0
 - IO4
 - RX
 - TX
 - SENV
 - VCC
 - VCC
- | | |
|-------|-----|
| J5 | GND |
| GND | GND |
| GND | GND |
| GND | GND |
| IO34 | |
| IO35 | |
| SENVN | |
| VCC | |

U2

CLK D0 D1 C 15 2 4 16 17 18 19 GND 21 RX 1X 22 23 GND

303 EN UN UN 34 35 32 33 25 26 27 1 12 GND 13 02 DS CHD BU

U1

C1

C2

U1

IDT™
7132
SA100P
S1240P

C1

C2

J1

J3

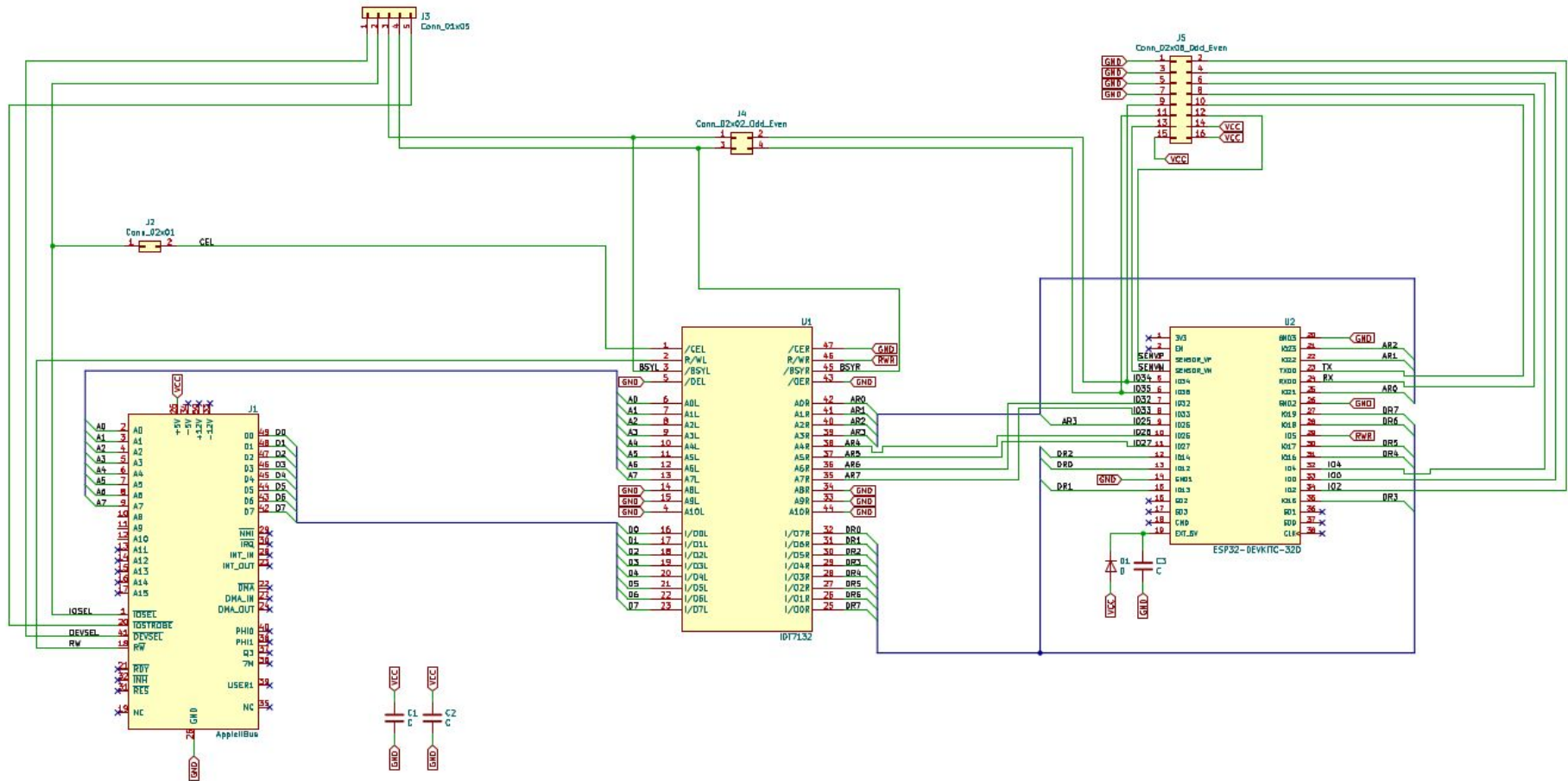
IOSEL
BAK-CEC

J4

IOSEL
IOSEL
BSYL
BSYR
IOSTROBE

J5

BSYL
BSYR



LIST

```

J      C = 0
10     M = 0
20     PR1 = 49312
30     PR2 = M TO M + 15 STEP 1
40     PEEK (N)
50     PEEK (N)
60     PRINT N, PR1, PR2
70     C = C + 1
80     NEXT N
J

```



90 NEXT N

150 POKE N,R1+R1

1RUN

ADDRESS

499

499

499

499

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DATA

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DATA'

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499

1*

On to the Software

apple2idiot

IDT7132 RAM

Write Data

Address: Data: Option:

Memory Map

ADDRESS	DATA
49312	255
49313	0
49314	1
49315	2
49316	3
49317	0
49318	42
49319	27
49320	111
49321	188
49322	199
49323	55
49324	0
49325	0

IRUN CSCANWIFI

IRUN SCANWIFI

AP #	ACCESS POINT
1	GSO
2	DIRECT-0A-HP OfficeJet
3	Pro 8020
4	GSO

SELECT WIFI AP #: 1
PASSWORD (BLANK IF NONE): Test1234

IRUN SHOWIP
192.168.1.121

I#

LONDON/UK few clouds

TEMP: 289.57K
HUMIDITY: 82%
WIND SPEED: 5.14 m/s

MENU

- (1) COUNTRY
- (2) CITY
- (3) FETCH WEATHER
- (4) SHOW WEATHER
- (0) QUIT

UK
LONDON

SELECT :

COUNTRY CITY FETCH DISPLAY QUIT

COUNTRY: MX CITY: MEXICO CITY

MEXICO CITY (MX)

TEMP: 294.23 K

HUMIDITY: 47%

WIND SPEED: 1.91 M/S

WIND DIR: 21

SUMMARY: CLOUDS, OVERCAST CLOUDS

MENU SELECTION:

IRUN SLACK

-
- (1) SET CHANNEL
 - (2) SEND MESSAGE
 - (3) GET MESSAGES
 - (4) SHOW MESSAGES
 - (0) QUIT

Current channel:

SELECT: 1
CHANNEL NAME: general

-
- (1) SET CHANNEL
 - (2) SEND MESSAGE
 - (3) GET MESSAGES
 - (4) SHOW MESSAGES
 - (0) QUIT

Current channel: general

SELECT: 2
MESSAGE: This message is sent from my Apple //e using the apple2idiot card.█

FROM ESP: LOCAL GAME \ SETTINGS \ QUIT
AI MOVE: D8F6

CON YOU WIN
D8F6
D
C8F6
D8F6
E8F6
D8F6
E8F6

YOU LOSE.
(PRESS A KEY)

YOUR MOVE: c1b2 ✓



LONGITUDE: 155.0000
LATITUDE: 19.0000
DATE: APR 4 11:42:11
TIME: 100%
MODE: 014


```
App loop: 0
Checking ID: 202
App loop: 1
Checking ID: 200
Received a command for ISS()
ISS() handleCommand
ISS() COMMAND_GET_ISS
WRITE: 6 -> 0
ISS() before fetch_iss()
  http://api.open-notify.org/iss-now.json
  After GET()
  httpCode:200
+++++++
{"iss_position": {"longitude": "-120.4488", "latitude": "-10.6903"}, "timestamp": 1658442399, "message": "success"}
+++++++
-----
{
  "iss_position": {
    "longitude": "-120.4488",
    "latitude": "-10.6903"
  },
  "timestamp": 1658442399,
  "message": null
}-----
{
  "longitude": "-120.4488",
  "latitude": "-10.6903"
}-----
...command for ISS() handled
```


So what is it?

- A very **general purpose** microcontroller expansion card..
 - Web APIs
 - Weather, Chess, D&D API, Plex controller, Google sheets importer for visicalc
 - Webserver or serial output for Apple II software debugging
 - Coprocessor for encryption
 - Sensors, ADC, MQTT/IOT
 - Adhock network chat/games
 - Bluetooth
 - NTP -> Prodos time
- ...That becomes a very **specific purpose** card once you put the firmware on the ESP32.

Pros and Cons

- Pros
 - Easy and inexpensive to build at home. Low chip count. Through hole components.
 - Card handles hard stuff (e.g. JSON parsing, https)
 - Easily hackable
- Cons
 - To do something, you have to write code for Apple II and ESP32.
 - Card has to have the correct firmware for the software you want to run.
- Maybe you should look at:
 - Fujinet
 - Uthernet II

Future?

- Multiplayer
- Eigengrau's Town generator + D&D API dynamic adventure game.

A bit about the ESP32

- Can be programmed with Arduino IDE... but also can be programmed with Espressif's c/asm toolchains, or, NodeMCU LUA.
- Pins can be a nightmare...

