```
        8                                    .d8
        8  d7                                8               8
        8 dP  ,8888 ,888. ,8887 ,8888 ,8887  888 .8887 ,8887 888
        888b  8   8 8   8 '"o,. 8   8 '"o,.  8   8  7  '"o,. 8.
        8" '8 "88 8 8   8 d888' "88 8 d888' .8   `8888 d888' `88
            8                              d8'
```

Apple IIgs Timing and the Fast Processor Interface

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OVERVIEW

The FPI goes by two names, depending on whether it's located in a ROM 1 or ROM 3 machine. This text uses the term FPI to refer to both variants.

FPI: Fast Processor Interface
CYA: Control Your Apple (Not according to Urban Dictionary)

The FPI is the interface between the legacy Apple II bus and the fast IIgs processor and memory.

It has Three Main (Interrelated) Duties:

1. Generate PH2, the fast CPU clock

2. Interface with fast RAM, ROM, and the slow bus

3. Control video RAM and I/O shadowing

PH2 GENERATION

The FPI is clocked by 14M, the same ~14MHz signal available in 8bit Apple IIs. Sequential outputs of the FPI are loaded on the rising edge of 14M. All intervals below are in units of 14M ticks (~70ns).

There are three types of PH2 cycles. One type, the SYNC cycle, may look slightly different depending on whether the slow bus is about to execute a STRETCH cycle or not.

Cycle	Low	High	Total
Normal Fast	2	3	5

Fast Refresh	2	8	10
Sync	2	12-25	14-27
Sync Stretch	2	14-27	16-29

In a NORMAL FAST cycle, PH2 is running at its fastest rate. This cycle is used for accesses to fast RAM and ROM, when the system speed is set to FAST. When accessing ROM, the fast RAM can also be refreshed during this cycle, incurring no speed loss.

In a FAST REFRESH cycle, the high phase of PH2 is extended by 5 ticks. A RAM refresh is performed in the first 5 ticks, followed by the normal access in the second 5 ticks. This cycle is used for accesses to fast RAM, when the system speed is set to FAST. When running completely from fast RAM, every 9th PH2 cycle is a FAST REFRESH cycle.

In a SYNC cycle, the high phase of PH2 is extended by as many ticks as are necessary to align with a full cycle of PH0. If the falling edge of PH2 coincides with the falling edge of PH0, then "only" 9 ticks must be added (11 ticks for a STRETCH cycle). If the falling edges do not align, then an additional 1 to 13 ticks are added to wait for PH0. Fast RAM can also be refreshed during this cycle, incurring no speed loss.

PH0 SYNCHRONIZATION

During a SYNC cycle, the FPI extends PH2 so that it is synchronized to PH0. However, PH0 is generated by the MEGA II and is not connected to the FPI! The FPI recreates PH0 internally using 14M and STRETCH, a signal generated by the VGC, or Video Graphics Controller.

The FPI will issue a SYNC cycle in the following circumstances:

1. The system speed is set to SLOW.

2. An enabled Disk II Slot Monitor has detected that a Disk II is currently being accessed.

3. The system is writing to shadowed video RAM.

4. The system is reading or writing to I/O (with a few exceptions).

5. The system is accessing any address in banks $e0 or $e1.

SYSTEM SPEED : The base system speed is controlled by one bit in the
.............: SPEED REGISTER. The speed can be set to FAST or NORMAL.

In addition to the base system speed, the FPI can keep track of accesses to Disk II hardware in slots 4-7. The firmware enables this feature for slots in which it detects Disk II firmware at startup.

Specifically, the FPI tracks the I/O locations which start and stop the drive motor. If the drive is spinning, then the system speed is forced to NORMAL.

:
SHADOWING : In order to keep compatibility with the existing 8bit video
...........: modes, all video generation circuitry is located on the slow bus. SHADOWING improves overall system speed by minimizing the number of accesses to slow RAM.

The MEGA II MAIN and AUX banks, which contain the video buffers, are seen by the CPU at banks $e0 and $e1. The real MAIN and AUX banks are located at banks $00 and $01. When a SHADOWED write occurs, the system is slowed to NORMAL speed, and BOTH the fast RAM and MEGA II RAM are written to. All reads to SHADOWED memory occur at FAST system speed, since the data can be read directly from fast RAM.

SHADOWING can be enabled independently for most video buffer address ranges.

As a consequence of this arrangement of RAM banks, the FPI must also SHADOW accesses to I/O locations. 8bit applications expect to access I/O in banks $00 and $01. The bit which enables I/O SHADOWING also enables LANGUAGE CARD behavior in SHADOWED fast RAM banks. As a consequence, the FPI must implement all LANGUAGE CARD and AUX RAM softswitches.

Both reads and writes to I/O locations are SHADOWED, with the following exceptions:

1. Registers that exist only in the FPI are not SHADOWED at all. Both reads and write occur at FAST system speed.

   SHADOW, SPEED, and DMA

2. Registers that exist both in the FPI and MEGA II are SHADOWED during writes only. Reads occur at FAST system speed.

   SLOT, and STATE

Finally, SHADOWING can be enabled either for ALL fast RAM banks, or just banks $00 and $01. Most of the time, just banks $00 and $01 are SHADOWED. Only NinjaForce likes to SHADOW all banks...

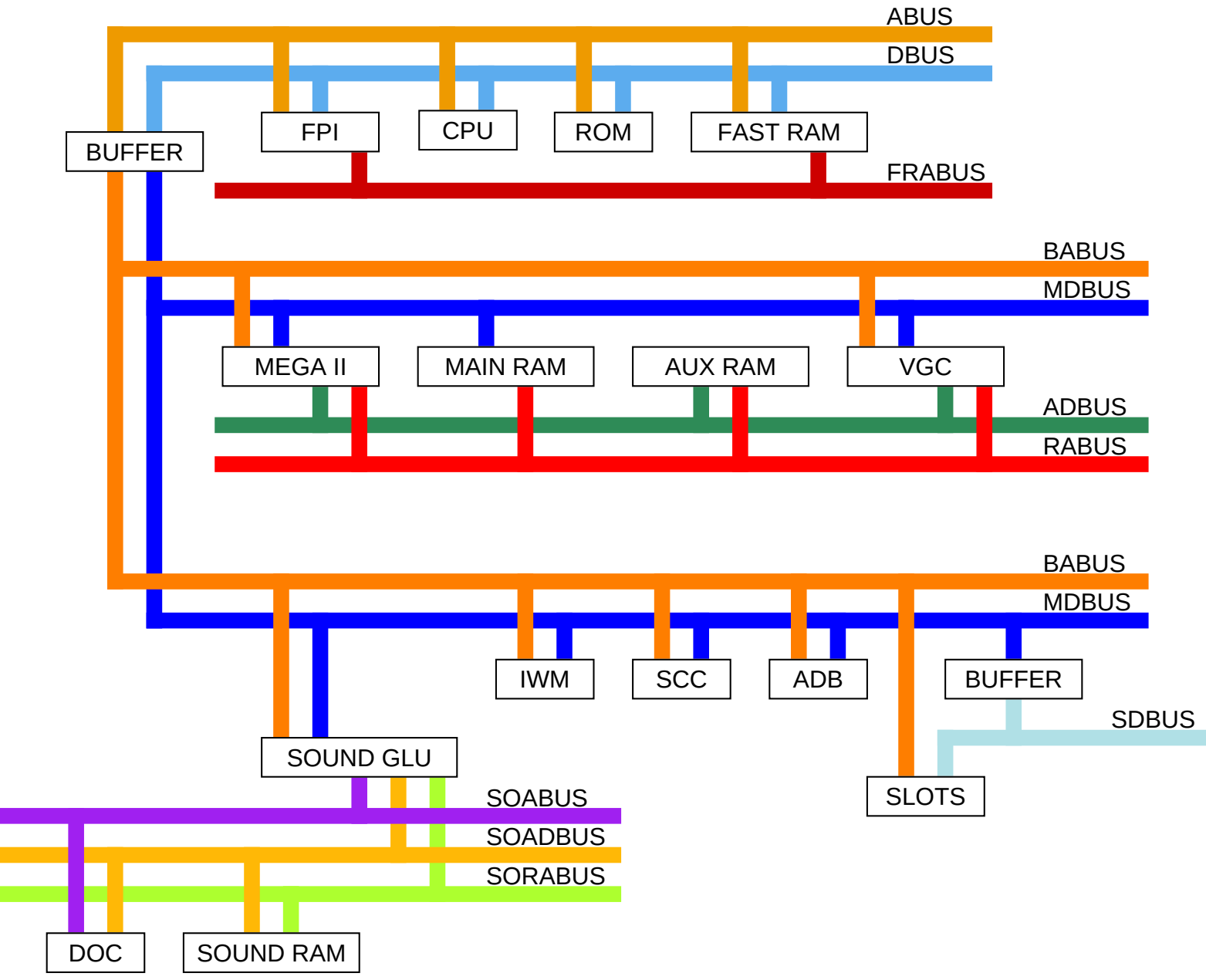
MEGA II INTERFACE

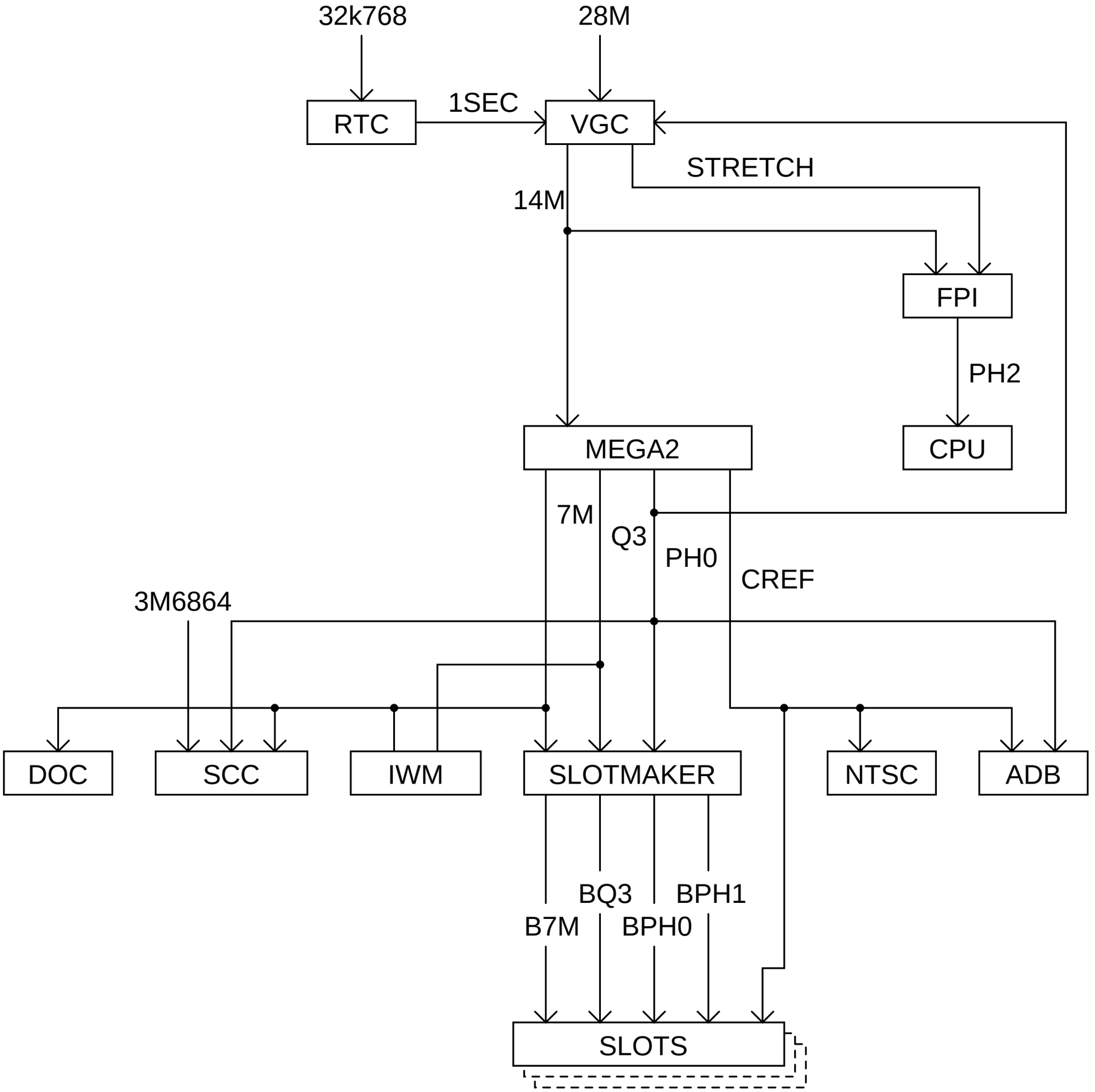
The slow and fast busses are connected via two buffers: one for the address signals and one for the data signals. Each buffer has two inputs which control whether it is enabled at all, and if so, which direction to transfer the signals.

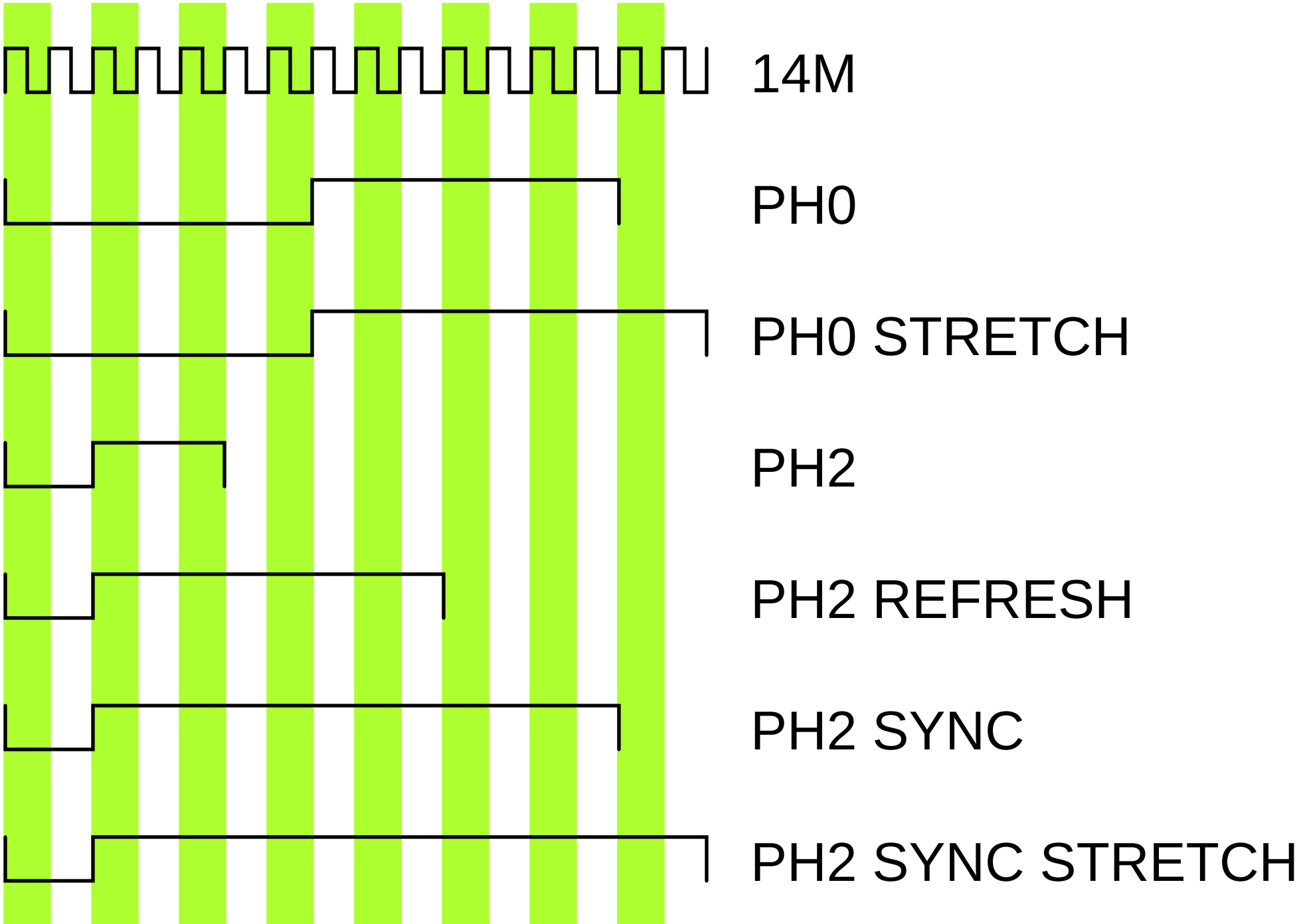
With the exception of DMA transfers, the address buffer is always enabled and configured to transfer from the fast to the slow side.

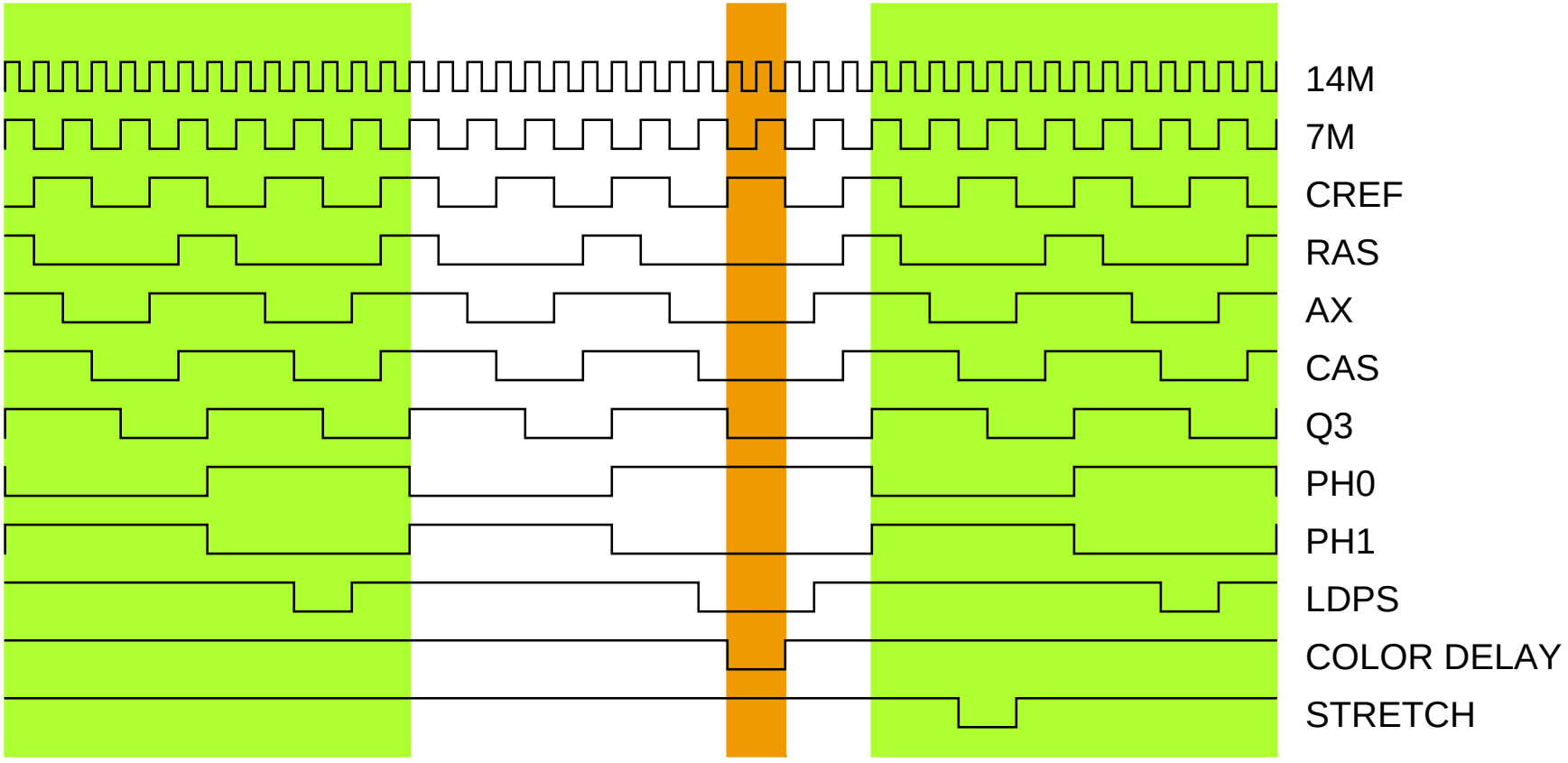
The data buffer is enabled on the second half of each slow cycle when PH0 is high. The video scanner has control of the slow bus during the first half of each slow cycle when PH0 is low. During a FAST cycle, the data buffer is always configured to transfer from the fast to the slow side. During a SYNC cycle, the data buffer direction depends on whether the operation is a read or a write. DMA transfers reverse the direction of this buffer, allowing peripheral cards access to fast RAM and ROM.

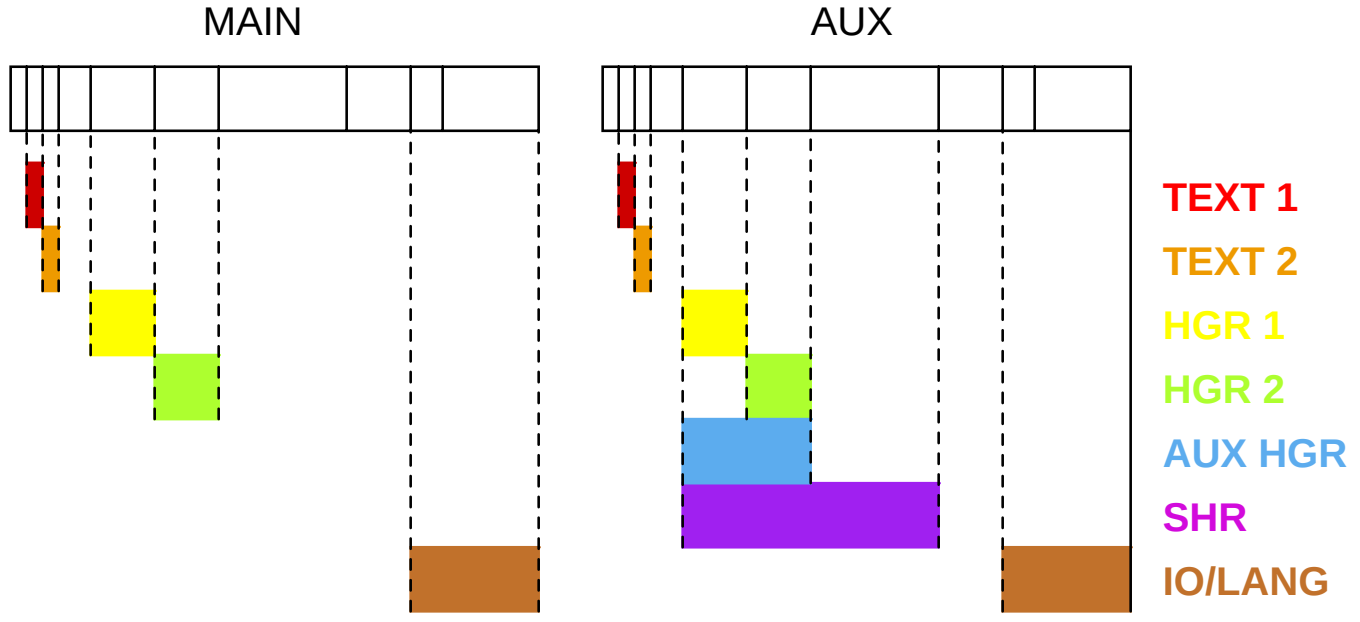
Both buffers drive the slow bus even during FAST cycles! All circuitry on the slow bus must check the M2SEL signal to determine when a SYNC cycle is in progress. The FPI asserts M2SEL during the portion of each SYNC cycle which overlaps a complete PH0 cycle.

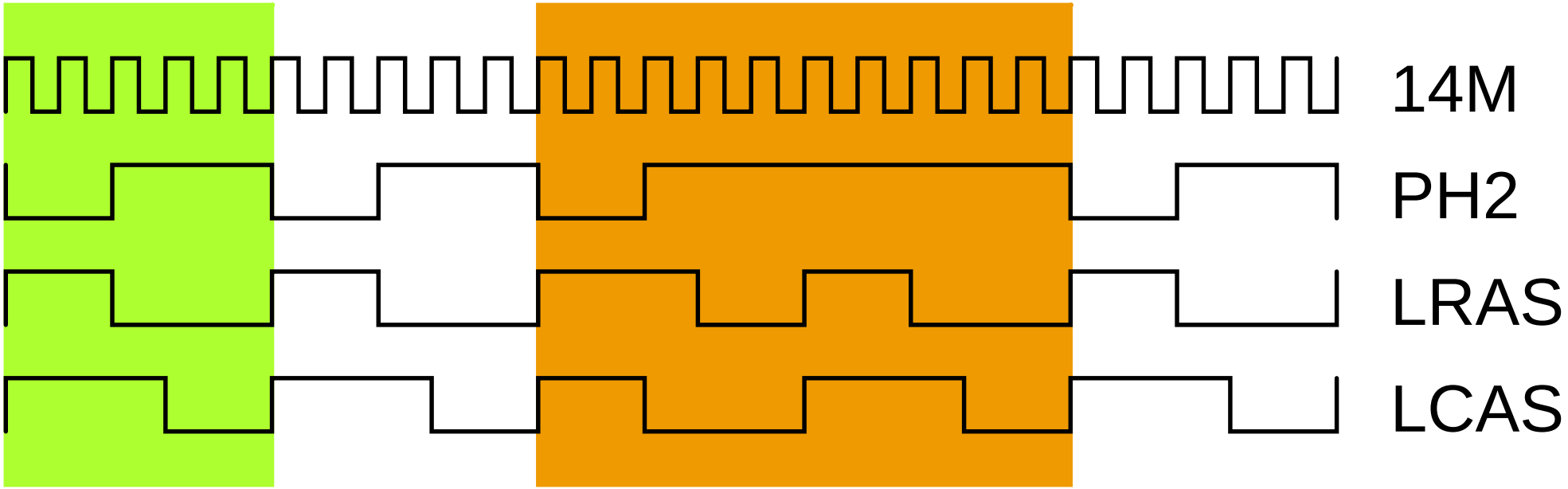

ABUS
DBUS
BUFFER
FPI
CPU
ROM
FAST RAM
FRABUS
BABUS
MDBUS
MEGA II
MAIN RAM
AUX RAM
VGC
ADBUS
RABUS
BABUS
MDBUS
IWM
SCC
ADB
BUFFER
SDBUS
SOUND GLU
SLOTS
SOABUS
SOADBUS
SORABUS
DOC
SOUND RAM

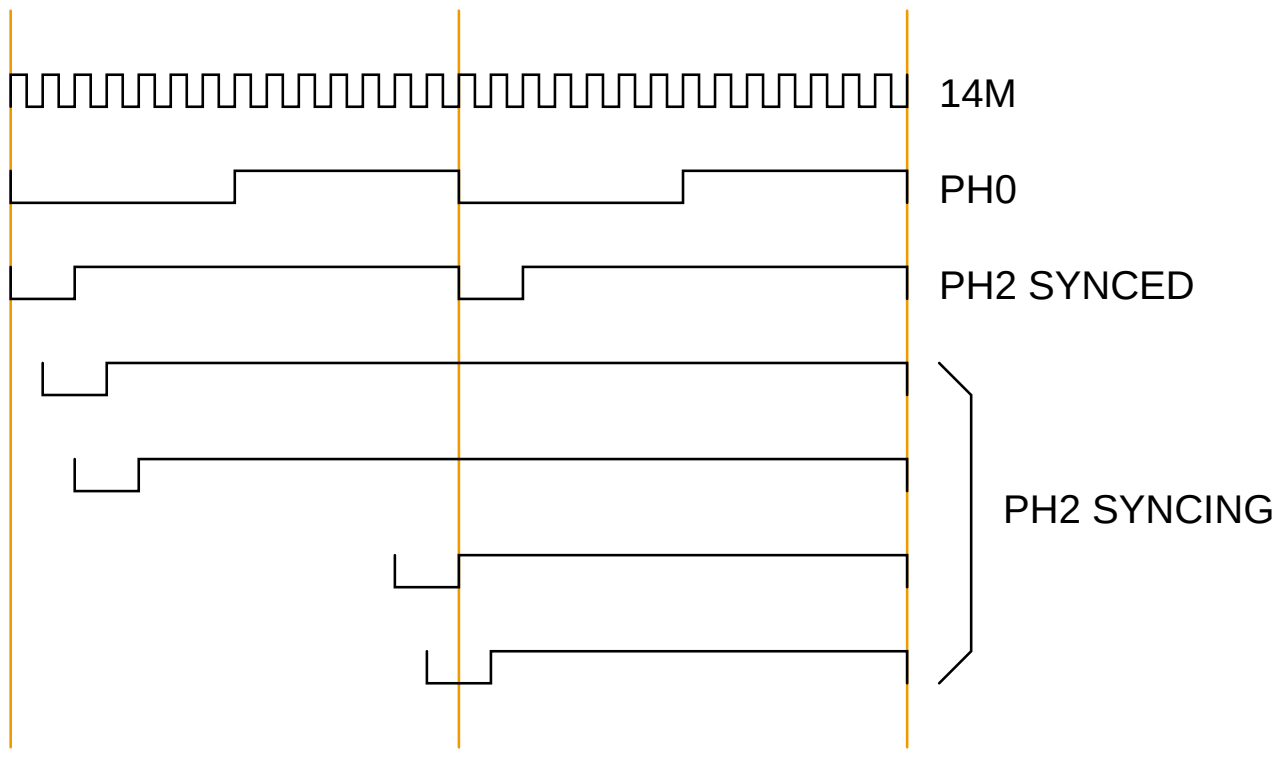

32k768
28M
RTC
1SEC
VGC
STRETCH
14M
FPI
PH2
CPU
MEGA2
7M
Q3
PH0
CREF
3M6864
DOC
SCC
IWM
SLOTMAKER
NTSC
ADB
BQ3
BPH1
B7M
BPH0
SLOTS


14M
PH0
PH0 STRETCH
PH2
PH2 REFRESH
PH2 SYNC
PH2 SYNC STRETCH


14M
7M
CREF
RAS
AX
CAS
Q3
PH0
PH1
LDPS
COLOR DELAY
STRETCH


MAIN
AUX
TEXT 1
TEXT 2
HGR 1
HGR 2
AUX HGR
SHR
IO/LANG


14M
PH2
LRAS
LCAS


14M
PH0
PH2 SYNCED
PH2 SYNCING